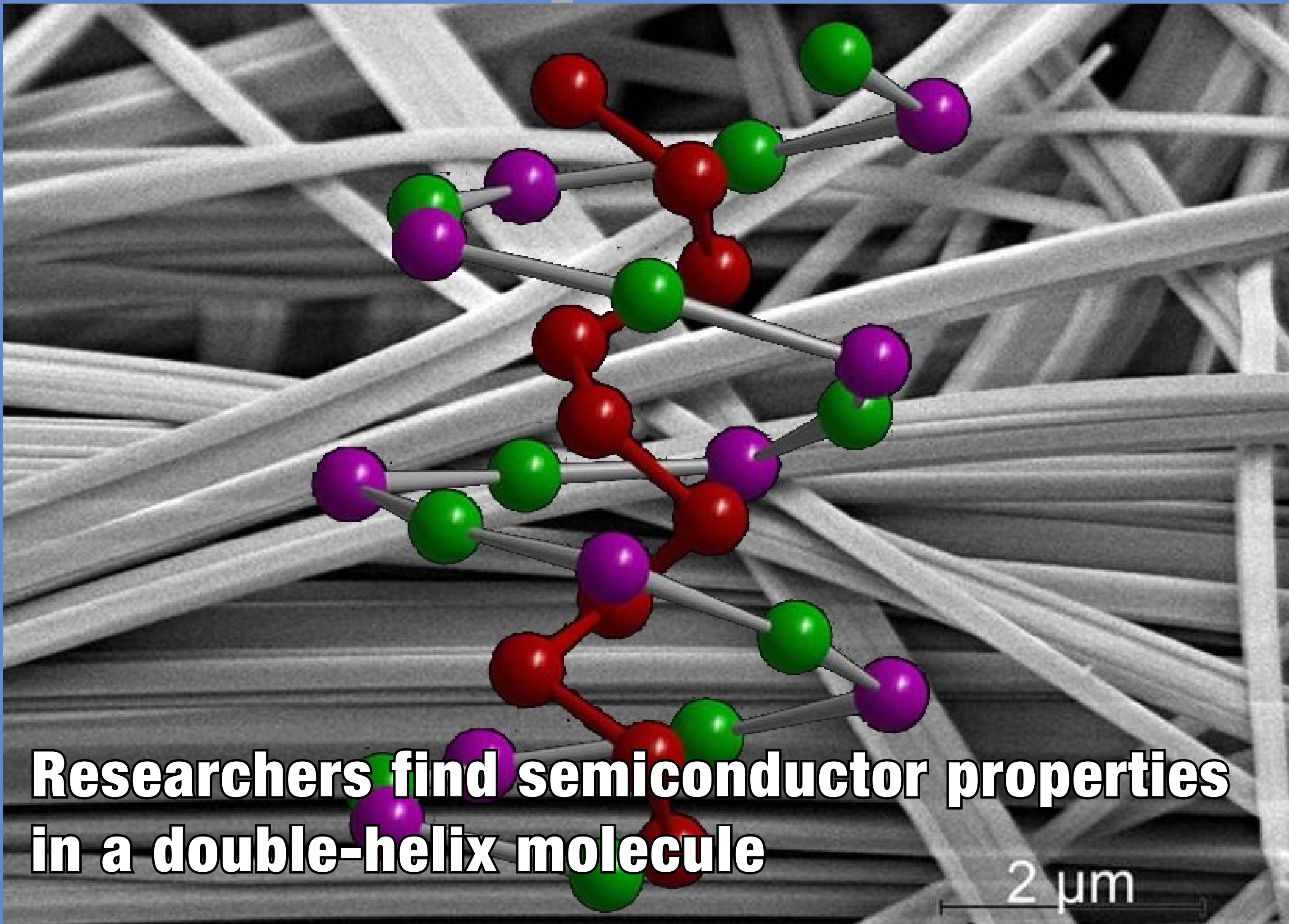
EDN europe

OCTOBER 2016

www.edn-europe.com



Researchers find semiconductor properties in a double-helix molecule


ONE. STOP. SHOP!
Best in Class: Helping You Innovate!
TOP OF MIND...*
#1 Semiconductors
#1 Interconnects
#1 Passives
#1 Electromechanical
#1 Automation & Control
#1 Power
#1 Test & Measure
#1 Easy to Navigate Website
#1 Website Checkout Process
#1 Data & Product Selection Support
#1 Broadest Overall Product Selection
#1 In-Stock for Immediate Shipment
#1 Consistent On-Time Delivery
#1 E-Commerce/Online Buying
#1 Website with Valuable Content for Design Support
#1 Design & Engineering Services
#1 Knowledgeable Sales Reps
#1 Online Technical Education & Training
Digi-Key ELECTRONICS
FIND CONTACT AND ORDERING INFORMATION FOR YOUR REGION AT
DIGIKEY.COM/EUROPE
*AspenCore's 11th Design Engineer and Supplier Interface Study gathered information from engineers regarding their need for product information and other services, as well as how and when they interface with suppliers and how they see the quality and value of that interface. 1,750 U.S. engineers participated in this year's web-based survey. The results represent those surveys completed by April 2016. Rankings reflect results among the industry's electronic component distributors.
AspenCore
Digi-Key is an authorized distributor for all supplier partners. New products added daily. © 2016 Digi-Key Electronics, 701 Brooks Ave. South, Thief River Falls, MN 56701, USA
ecia MEMBER
ecsn member
CEDA

COVER

A double helix in inorganic chemistry – and it's a semiconductor

Researchers from the Technical University of Munich (TUM) have synthesized an inorganic semiconductor material, SnIP, whose highly flexible strands feature a double helix structure. In the composite image on this month's cover, the background is a micrograph of the fibre or needle form of the material that the Munich researchers have synthesised; the superimposed molecular model represents its structure. One chain of the double helix is formed by an alternating string consisting tin and iodine atoms, the other is formed by phosphorus atoms. The novel semiconductor exhibits extraordinary optical and electronic properties, as well as extreme mechanical flexibility, with centimetre-long fibres that can be arbitrarily bent without breaking. The thinnest SnIP fibres to date comprise only five double helix strands and are only a few nanometres thick.

"This property of SnIP is clearly attributable to the double helix," says Daniela Pfister, who discovered the material and works as a researcher in the work group of Tom Nilges, Professor for Synthesis and Characterization of Innovative Materials at TU Munich. "SnIP can be easily produced on a gram scale and is, unlike gallium arsenide, which has similar electronic characteristics, far less toxic."

Through appropriate doping, the researchers expect the novel material to lend itself to many applications in the electronic industry, from energy conversion in solar cells and thermoelectric elements to photocatalysts, sensors and optoelectronic elements. Full item here.

FEATUREARTICLES

ONLINE THIS MONTH

Generate PAM4 signals for receiver compliance testing

Resets in FPGA & ASIC control and data paths

Using low voltage precision op amps for a high voltage sensing application

EDN's columns

TASK PRIORITISATION

A headline from a UK daily newspaper in September; "Touchscreens in cars will cause road deaths to soar".

The article that ran under this headline cited some forthcoming model features – notably LCD panels "the size of a small television" on the fascias of high-end models and, increasingly in mid-range cars as well. It then noted the intention to connect these screens, either to a smartphone, or via embedded cellular link, to the wider world of social media. Connectivity, it appears, is now an absolute must-have in the automotive feature set. The reporter had sought comment from a number of road safety organisations which, predictably enough, feared a sharp upturn in accidents due to driver distraction. A spokesman for one such organisation was quoted saying, "Sadly the marketing people and not the safety people are in the driving seat..." - a statement with which this engineering audience might have some sympathy.

Let's set aside for a moment the fact that the main concern of many readers of these pages will be to implement such a scheme, and not to worry about misuse of their handiwork. The basic premise that an increasing range of connected facilities in the car, that are accessible to the driver, constitutes a safety hazard, is difficult to refute.

The issue is a continuation of the problem that arose with cellphones, and the subsequent legislation enacted in most countries and territories to prohibit the use of hand-held phones while driving. One view of the issue is that, at root, it is a training problem. Being able to maintain a verbal exchange while carrying out a physical task (such as driving) is clearly not impossible; if it were, commercial aircraft would be in trouble on a regular basis. The differentiating factor is that pilots are explicitly trained to give maximum attention to the most important part of their workload (flying the aircraft) and to give lesser importance to subsidiary matters (such as communicating). To express it in software coding terms, this is a task prioritisation issue; and as the aviation case suggests, it is a teachable skill – but one which (mostly, at least) does not feature in driving training.

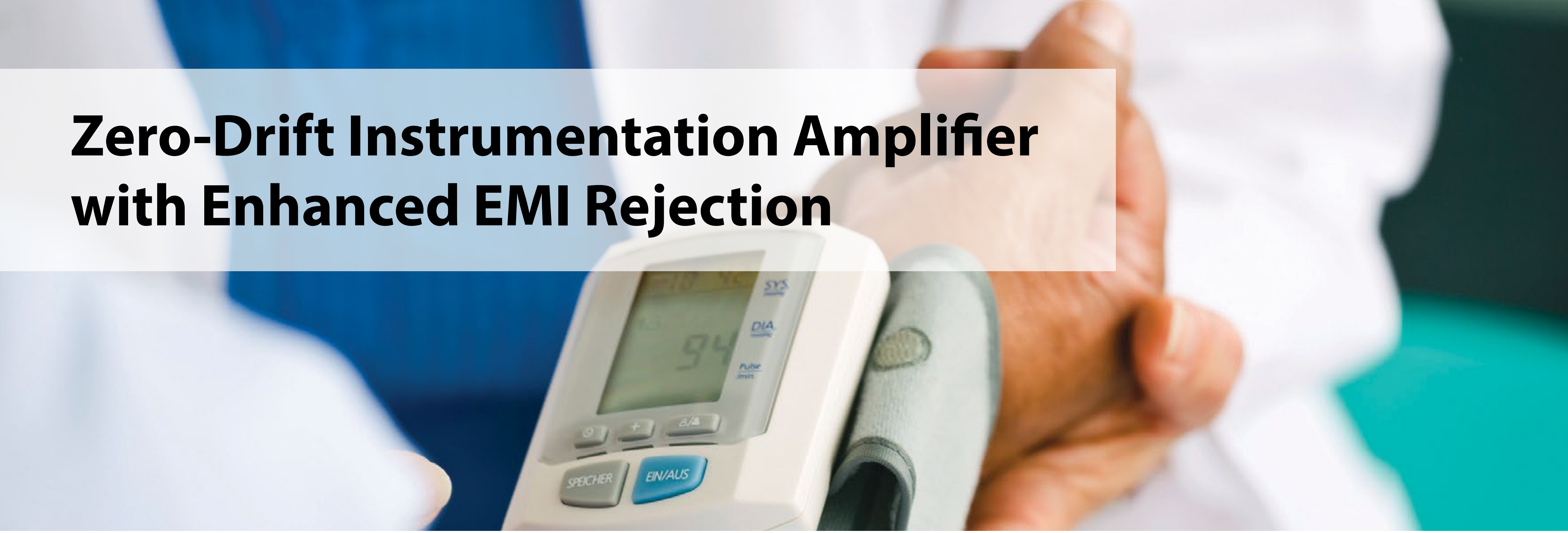
As model-year 2017/18 cars come to the market, a combination of factors may converge to make the – apparently alarmist – newspaper headline, a reality. Larger, more attention-grabbing screens are now a marketing must-have, and there appears to be relatively little control on what apps are able to appear at any time – social media alerts not excluded. Layered on to that is the fact that we (or at least, those of us who are heavy social media users) are increasingly conditioned to respond to smart-phone "interrupts" - to extend the coding analogy further – as a highest-priority-level event. Police forces struggle to enforce even the "no-hand-held" rule; there is little chance of them intervening to stop drivers turning their attention to incoming posts or tweets – even if efforts have been made to keep that class of traffic away from the driver.

To express that another way; we have created the toys of the fully-autonomous car, well before that much-discussed concept is anywhere close to being a reality. Technology may have created this problem, but it's a human-factors matter now, and technology fixes are of limited value. We can, for example, install a dual-view screen so that the content is invisible to the driver; but the distraction factor for those conditioned to scan every Tweet is hardly diminished.

Other gadget-centric fixes for the problem of conveying information to the driver include fitting head-up displays. The underlying assumption being that if you can avoid diverting the driver's gaze from the road ahead ("taking eyes off the road") you have solved the problem of distraction. This could be far from true. The real concern is where the driver's attention, and not necessarily his or her line of sight, is focused.

Was the newspaper article alarmist? I'm not at all confident that it was; what do you think?

Graham Prophet, edn-editor@eetimes.be



Zero-Drift Instrumentation Amplifier with Enhanced EMI Rejection

The MCP6N16 Instrumentation Amplifier provides superior DC performance including low off set voltage, low offset voltage drift, no 1/f noise and high common mode and power supply rejection. In addition, the device supports rail-to-rail operation on both the input and the output across an operating voltage range of 1.8V to 5.5V. Other valuable features include the closed loop gain being set via two external resistors maximizing the ability to control gain accuracy across temperature and the built in EMI rejection capability reducing errors caused from external sources of electromagnetic interference. The MCP6N16 Instrumentation Amplifier is ideal for interfacing to real-world sensors in applications monitoring temperature, pressure, strain, flow and vibration just to name a few.

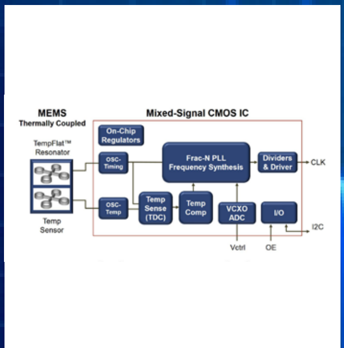
MCP6N16 Evaluation Board (ADM00640)

- Ultra-high precision
- On-chip EMI filtering
- Low voltage/low current operation
- Rail-to-rail performance

microchip DIRECT
www.microchipdirect.com

MICROCHIP
www.microchip.com/MCP6N16

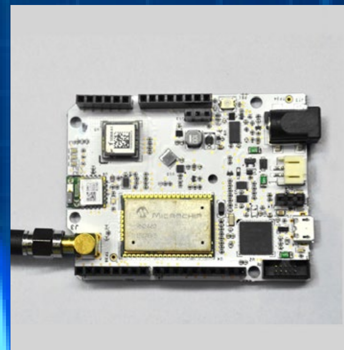
pulse

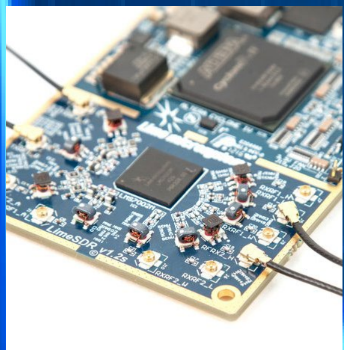


MEMS
Thermally Coupled
Mixed-Signal CMOS IC
TempFlat™ Resonator
On-Chip Regulators
OSC-Timing
Frac-N PLL Frequency Synthesis
Dividers & Driver
CLK
OSC-Temp
Temp Sense (TDC)
Temp Comp
VCXO ADC
I/O
I2C
Temp Sensor
Vctrl
OE

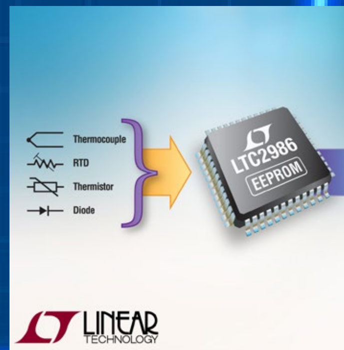
intersil
ISL79985
ISL79986

LoRa™ and ultra-low-power
STM32 Nucleo Pack
LoRa





C2
C20
R22
D2
HALO
TGSP-
P153EP13
1609LF



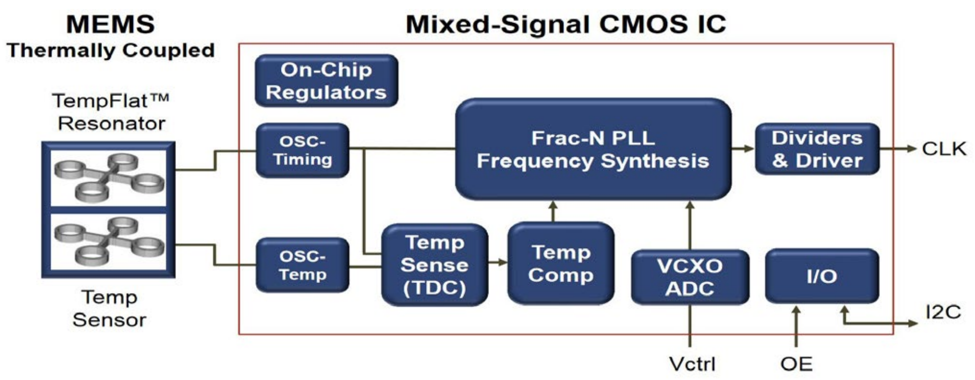
Thermocouple
RTD
Thermistor
Diode
LTC2986
EEPROM
LINEAR TECHNOLOGY

smartbond
TV

MEMS oscillators exceed quartz performance for comms, network timing

SiTime (Sunnyvale, California) is a designer and supplier of oscillators and timing products based on micro-machined mechanical resonating elements rather than piezoelectric devices (quartz). The company has, over several years, gradually been improving the stability of the MEMS devices it makes, to challenge the role of quartz in an increasing portion of the market.

Now, SiTime has introduced its Elite platform of oscillators. It continues to use the terminology "TCXO" (the X originally stood for 'crystal') as it is in widespread use, but the Elite devices are entirely MEMS-based. They are temperature compensated by use of a dual-resonator structure and by stored parameters, but claim levels of stability that can exceed those of quartz, when quartz is operated in a stable temperature, heated, environment (oven, or OCXO). With the Elite range, SiTime aims to capture a wider range of timing functions in telecoms and networking, offering performance gains in overall stability, in stability over temperature change, and in resistance to frequency change with mechanical shock or vibration ("microphony"). The company sets out the progress that MEMS-based parts have made over approximately the last decade; stability has gone from around 25 ppm to 0.1 ppm with the Elite products; a company spokesman attributes the greater part of this progress to optimising the compensation techniques applied to MEMS technology, and perhaps 40% to improvement in the basic fabrication technology. Jitter (short-term stability) has gone from 175 psec to 0.23 psec over the same time span.



The Elite Platform comprises four product families with a wide range of frequencies; all offer 0.1 ppb/g vibration immunity and do not have activity dips or micro-jumps. The immunity to vibration is particularly important where high stability is required in, for example, a cell site located in a noisy environment such as road or industrial vibration. The family comprises; Stratum 3 precision Super-TCXOs aimed at communications and cloud infrastructure; Super-TCXOs for GNSS, industrial and automotive applications; Ultra-low jitter differential oscillators; and High-temperature high-reliability differential VCXOs.

Complete article, here

Rad-hard FPGAs feature in Juno probe control and instrumentation

Microsemi has disclosed that a 'wide variety' of its radiation-tolerant products are employed in mission-critical applications on the Juno spacecraft currently in Jupiter orbit, and continue to support the historic mission in the hostile, intense radiation environment around Jupiter. *(Illustration courtesy NASA, www.nasa.gov)*

Saluting NASA on the successful mission as it progresses towards data collection phase, Microsemi cites the presence of its radiation-tolerant field programmable gate arrays from the RTSX-SU and RTAX-S product families in use within the space vehicle's command and control systems, and in various instruments which have now been deployed and are returning scientific data. Microsemi's high and low voltage radiation-hardened power supply modules support guidance and controls systems on board the Juno spacecraft.

Complete article, here

ARM reveals R52 core for 'highest functional safety standards'

ARM has headlined its latest processor core IP announcement as "enabling autonomous vehicles" but this is "today's spin" on a core with safety features that are applicable across automotive, medical and industrial sectors. Cortex-R52, based on the ARMv8-R architecture, has been designed to address functional safety in systems that must comply with ISO 26262 ASIL D and IEC 61508 SIL 3, in the automotive and industrial markets.

The core will, ARM says, have the real-time performance needed for next generation autonomous systems, while simplifying safety certification of automotive, industrial and medical applications, such as surgical automation, safety management and automotive powertrain control. STMicroelectronics is the first ARM partner to announce it has licensed the high performance processor to enable it to create highly integrated SoCs for the automotive market.

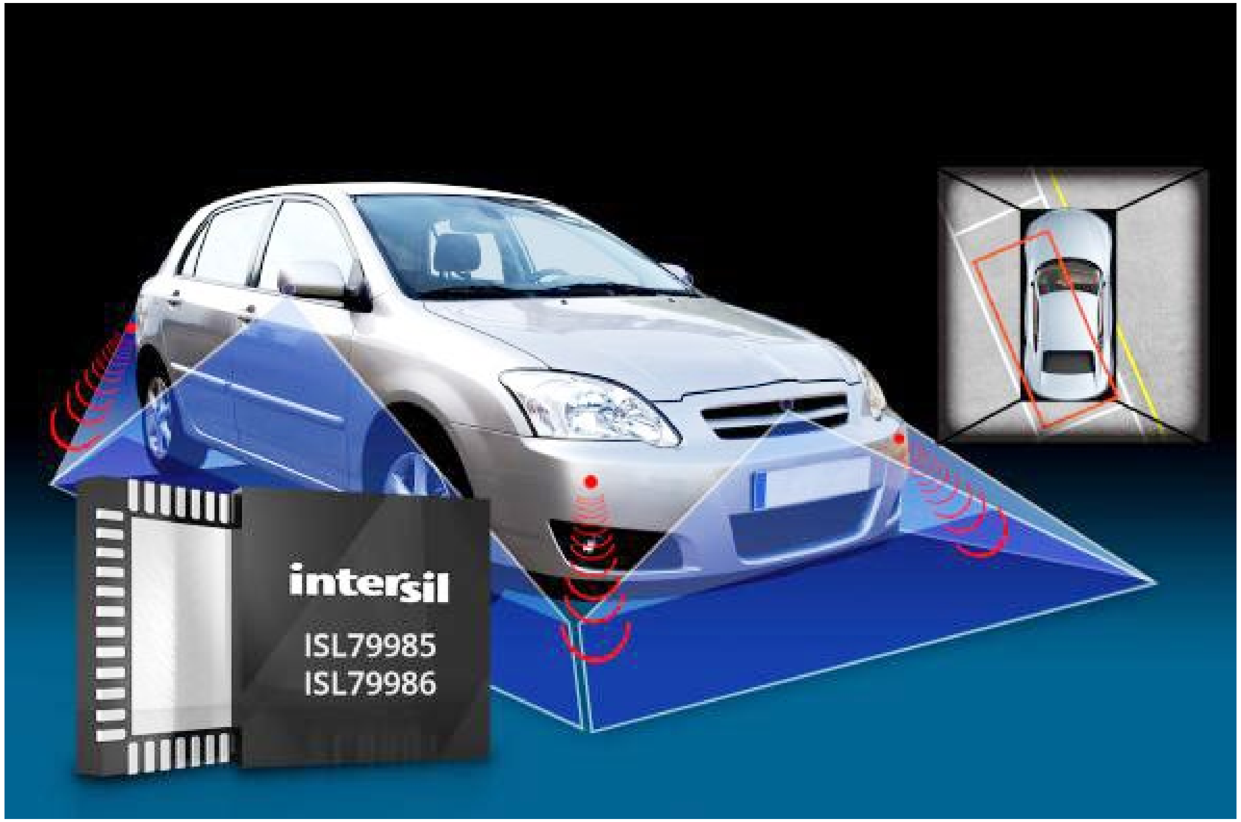
The Cortex-R52 employs hardware-enforced separation of software tasks to ensure safety-critical code is fully isolated. This allows the hardware to be managed by a software hypervisor policing the execution and resourcing of tasks. By enabling the precise and robust separation of software, the Cortex-R52 decreases the amount of code that must be safety-certified, so speeding up development as software integration, maintenance and validation is easier. The processor also deals with increased software complexity while delivering the determinism and fast context switching.

ARM Fast Models and Cycle Models are available for software partners to get access to the Cortex-R52 early in the design process. The Cortex-R52 claims a 35% performance uplift compared to the Cortex-R5, which has been deployed in a range of safety applications. The R52 has achieved a score of 1.36 Automark/MHz on the EEMBC AutoBench, the highest in its class, using the Green Hills Compiler 2017. Green Hills Software is expanding its support for ARM processors with optimizing compiler solutions for the Cortex-R52.

Complete article, here

4-ch video decoder for automotive surround-vision has MIPI-CSI2 interface

Intersil's ISL79985/86 parts are four-channel analogue video decoders that are configured to route camera feeds to image processors in automotive vision systems. The -85 part has a MIPI-CSI2 interface (parallel-bus interfaces have been standard in this context); the -86 device multiplexes all four camera feed on to a 4x speed, 8-bit bus. These parts continue the family of vision-oriented devices that Intersil acquired when it purchased Techwell in 2010. Intersil itself is now to be acquired by Renesas (see Renesas to acquire Intersil; aims to be #1 in embedded solutions); which is not the first time that the Intersil name will have been absorbed into another entity. The original Intersil was taken over by Harris; Harris resurrected the brand when spinning out the semiconductor operation, once again, in 1999.

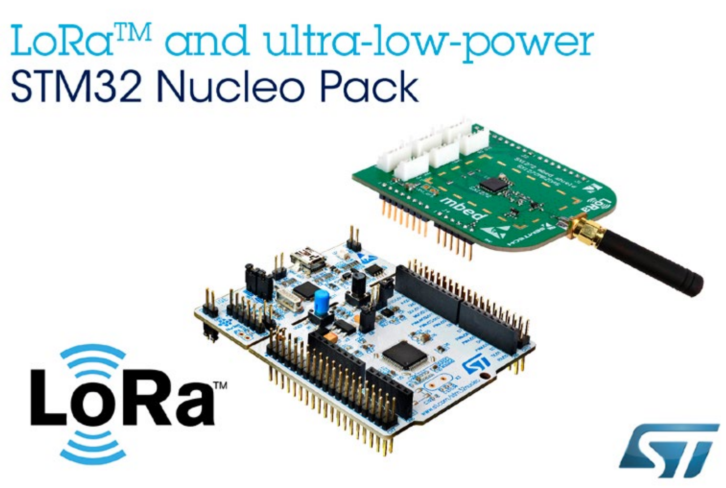


One of the immediate drivers for this update of vision processing components is the requirement that by model year 2018, all vehicles in the US must have reversing ("back-up") camera systems. One parameter of this specification is that the rear-view camera systems must boot-up quickly, in less than 2 seconds, so that the reversing image is available immediately to the driver upon starting the car. This is implemented as part of the function envisaged for the integrated ISL79985, which generates a 360-degree birds-eye-view, quality image for advanced driver assistance systems. It is positioned as the first four-channel analogue video decoder with MIPI-CSI2 output interface that supports the latest generation of SOCs and application processors. The ISL79985 replaces up to nine discrete components with a single chip to preserve critical board space. The ISL7998x family also includes the new ISL79986 with a line-interleaved BT.656 interface, at a 108-MHz rate.

The ISL79985 and ISL79986 integrate four analogue video decoders with 10-bit ADCs to support four analogue camera CVBS inputs simultaneously. The ISL79985's MIPI-CSI2 interface lowers system EMI, reduces the number of pins compared to a traditional parallel interface, and makes it easy to interface with the newest SOCs and ADAS processors.

Complete article, here

ST's LoRa kit adds low-power radio to STM32 MCU scene



STMicroelectronics has a low-cost development kit that makes use of the STM32 microcontroller ecosystem for prototyping Internet-of-Things (IoT) devices with LoRa Wireless Low-Power Wide Area Network (LPWAN) connectivity. Priced at $40, the P-NUCLEO-LRWAN1 kit combines the ultra-low-power STM32L073 Nucleo (NUCLEO-L073RZ) microcontroller board with an RF expansion board based on the SX1272 LoRa transceiver from Semtech (I-NUCLEO-SX1272D). The STM32L073 MCU, with its ARM Cortex-M0+ core and proprietary ultra-low-power features, provides a host for devices such as utility meters, alarm systems, positioning devices, trackers, and remote sensors. Users can extend functionality by adding extra expansion boards, such as the X-NUCLEO-IKS01A1 sensor board for motion, humidity, and temperature sensing.

The new kit contains everything needed to build bi-directional end devices that comply with LoRaWAN version 1.0.1 and support class A and class C protocols. Devices can be activated using Over-The-Air Activation (OTAA) or Activation-By-Personalization (ABP). An application for LoRaWAN certification tests is included in the kit, and the I-CUBE-LRWAN LoRaWAN stack is available and posted at www.st.com/i-cube-lrwan.

Complete article, here

TI's STEM support for classroom engineering; the TI-Innovator Hub

Texas Instruments is introducing a classroom tool that puts the power of coding and engineering design into the hands of students.

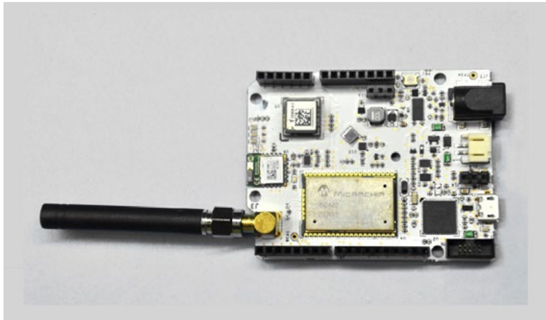
The TI-Innovator Hub is a palm-sized box with a built-in microcontroller, that plugs into the graphing calculator many middle and high school students already own, a TI-84 Plus CE or a TI-Nspire CX, and allows them to analyze and explain the world around them. It was created using the TI LaunchPad Board, the same technology used by engineers around the world to design cutting-edge products from smart watches to 3-D printers. For example, students can start by learning to write a program to play a single note, and then put together sounds at different frequencies to play a song.

TI has a multi-media product introduction page with video clips that further explain the concept, that you can find here.

Complete article, here

LoRa development board for long range IoT connectivity

Distributor Arrow Electronics has added to its own-brand range of board level products, extending support for developers of IoT products with the the SmartEverything LION board, providing a range of functions required in an IoT sensing node and enabling simple, low power connection to the Cloud via the LoRa protocol. The board was developed by Arrow Electronics in association with Axel Elettronica (Varedo, northern Italy) and is designed to simplify and speed the development processes for companies producing nodes for the IoT.



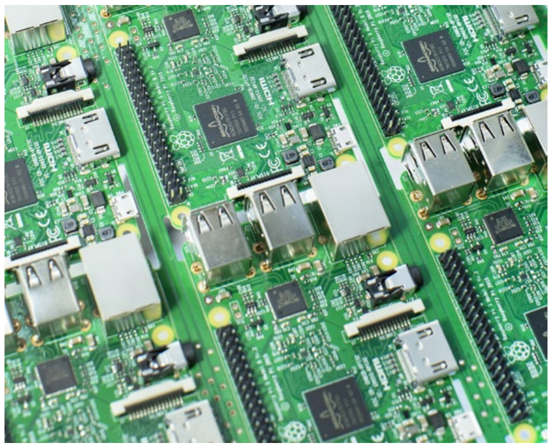
The LION board is based on the Arduino form factor and incorporates a Microchip LoRa module. It employs STMicroelectronics sensors for proximity, humidity, temperature and acceleration and includes a Microchip Bluetooth Low Energy interface for short-range connectivity, together with an external shield featuring NXP NFC Ntag I²C interface for authentication. Another external shield by Analog Devices is available with Temperature, precision Axis and Gas sensor for IOT applications. An Atmel ARM Cortex-M0+ based CPU USB Host orchestrator chip manages all traffic between peripherals. A Telit GPS with embedded antenna supports localization. Dynaflex 868MHz antenna and Linear Technology power management devices are also incorporated.

Complete article, here

Raspberry Pi hits 10million boards shipped

An event held at the UK Houses of Parliament on 8th September 2016 marked the shipment of the 10-millionth Raspberry Pi compute board, across all of the generations since its initial launch and conception as a tool for encouraging young minds to get into the coding mindset.

In their parallel roles as manufacturing partners and sales channels, distributors RS Components and Farnell element14 both participated in the event and issued their own comments marking the occasion; "RS Components [has] announced in conjunction with the Raspberry Pi Foundation that the cumulative sales total for Raspberry Pi products has now reached 10 million units, further cementing its position as the best-selling British computer ever.



RS has played an important role – from the very beginning in February 2012 - in enabling the Raspberry Pi to reach this impressive sales landmark. In addition to being an authorised distributor, RS is one of the official manufacturers of the Raspberry Pi and, during peak production, produces just short of 1400 boards per hour with manufacturing partner Sony at its factory in the UK."

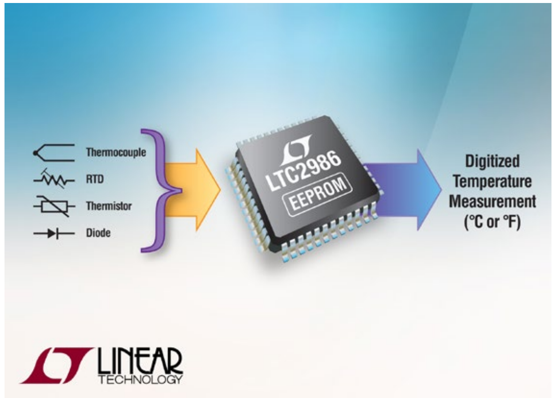
Farnell element14 similarly offers; "element14 has partnered the Raspberry Pi Foundation since 2012, has manufactured and sold over 6.5 million Raspberry Pis, and has an exclusive customization service for the Raspberry Pi for customers in industry."

To celebrate the milestone, Raspberry Pi has launched what it refers to as "the perfect bundle" which is available from RS Components, for £99/€125.10. The official Raspberry Pi Starter Kit contains a Raspberry Pi 3, a mouse and keyboard, an 8GB SD card with NOOBs operating system, an official Raspberry Pi case, a 2.5 amp power supply and a 1m HDMI cable. There is also an Adventures in Raspberry Pi book by Carrie-Anne Philbin.

Complete article, here

10-ch universal temperature measurement IC linearizes to 0.1°C

LTC2986 is a high performance digital temperature measurement IC, which directly digitizes any combination of thermocouples, RTDs, thermistors and external diodes with 0.1°C conformity and 0.001°C resolution. The LTC2986 builds on the (pin-compatible) LTC2983 and LTC2984 by adding three new operating modes and reducing the number of analogue inputs from 20 channels to 10 channels. The new operating modes provide better support for external overvoltage protection resistors that are shared between multiple sensor types, powered temperature sensors with analogue outputs, and other non-temperature related sensors such as pressure or other voltage output sensors. The IC's high performance analogue front end combines low noise and low offset buffered ADCs with all the necessary excitation and control circuits for each sensor. Measurements are performed under the control of a digital engine, combining all the algorithms and linearization required for each. The device precisely measures absolute microvolt level signals from thermocouples and ratiometric resistance measurements from RTDs and thermistors, performs the linearization and outputs the results in °C or °F. Up to ten analogue inputs are available, allowing support for up to nine thermocouples, four RTDs, four thermistors and/or ten diodes. The SPI interface works with virtually any digital system and a comprehensive software support system with drop-down menus allows easy customization of the LTC2986.

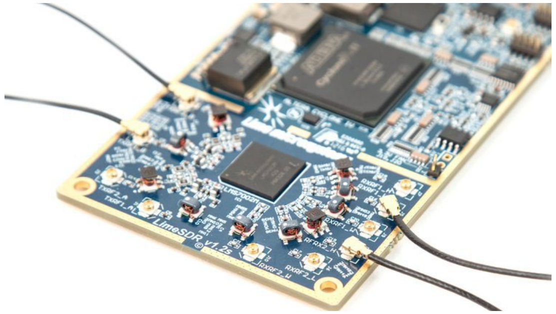


Complete article, here

Customized software defined radio chip for LimeSDR developers

LimeSDR, recently successfully funded on the Crowd Supply crowdfunding platform, is a low cost application-enabled software defined radio (SDR) platform that can be programmed to support virtually any type of wireless standard, from Wi-Fi, ZigBee and Bluetooth through to cellular standards such as UMTS, LTE and GSM and to the emerging IoT communication protocols such as LoRa.
Lime Micro has announced a manufacturing partnership for the LimeSDR product line with Advanced Semiconductor Engineering (Taiwan), provider of semiconductor packaging and testing services. Ebrahim Bushehri, CEO

of Lime Micro said, "We are very excited to partner with ASE and to offer the customized chip for the LimeSDR boards that were pledged during the campaign. It is testament to the excitement generated by the LimeSDR that ASE have agreed to partner with Lime and facilitate a customised run. The LimeSDR has had the ambition right from the beginning to transform wireless connectivity

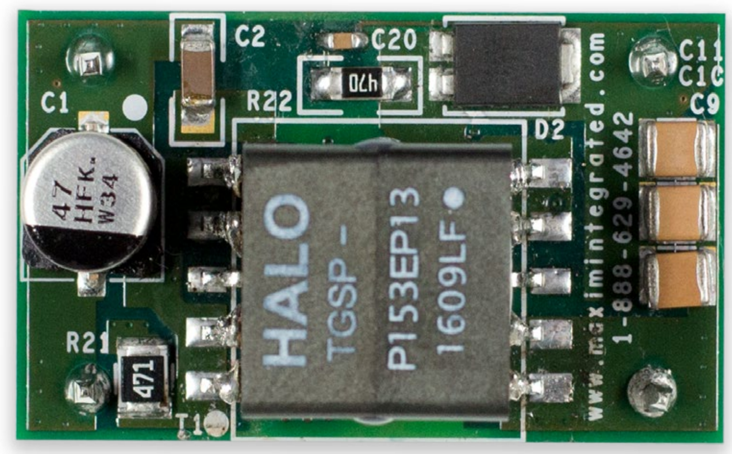


and develop an open community backed model for innovation. The endorsement of the community has been a major step in achieving this goal." Individual LimeSDR boards cost $289. Large 100-unit operator 'bundles' are also available through the campaign page as is a recently launched certification program.

Complete article, here

Maxim reference design sets out isolated 24V to 12V, 20W supply

Maxim has posted details of a series of isolated, industrial power-supply reference designs. Each of these power supplies efficiently converts 24V into useful voltage rails at a variety of power levels. Every power rail is isolated with a readily available transformer from multiple, global vendors, providing for quick, convenient transformer selection. Each design has been tested for load and line regulation, as well as efficiency and transient performance: BOM, schematics, layout files, and Gerber files are all available in the Design Resources tab. Boards are available for purchase; most boards feature through-hole pins for immediate board placement and accelerated prototyping. MAXREFDES113# is an efficient flyback topology with 24V input, and a 12V output at 20W of power (1.6A). The design features the MAX17596, a peak-current-mode converter with flexible switching frequency. This entire circuit fits on a 20 × 35mm board. A related design, MAXREFDES114, delivers 5V from 24V.



Maxim notes that, transformer selection is often the most difficult step in isolated power design. Multiple transformers (Halo Electronics TGSP-P153EP13LF, Wurth Electronics 750316112r01, HanRun HR051441, and Sumida 13324-T115) have been qualified for this design, simplifying the process of transformer selection. The reference design operates over a 17V to 36V input voltage range, and provides up to 1.6A (plus 20% overhead) at 12V output. The MAX17596 has an internal amplifier with 1% accurate reference, eliminating the need for an external reference. The switching frequency is programmable from 100 kHz to 1 MHz with an accuracy of 8%, allowing optimization of magnetic and filter components, resulting in compact and cost-effective power conversion. This design is set to switch at 200 kHz. For EMI-sensitive applications, the MAX17596 incorporates a programmable frequency dithering scheme, enabling low-EMI spread-spectrum operation.

Complete article, here

Configurable power supply outputs up to 1200W from 1U profile

XP Power's nanofleX series of configurable digitally controlled AC-DC power supplies has a compact low profile 1U mechanical chassis format that suits today's space constrained designs and can accommodate up to four single-slot plug-in customer selected output voltage modules. Designed to maximize efficiency and minimize audible fan noise, the nanofleX series can deliver up to 850W from a universal input voltage or up to 1,200W from a high line source. The four output module slots provide nineteen nominal output voltage options in the range + 3.3 to + 60 VDC. Outputs are derived from one of four base, digitally controlled, modules that each span a wide voltage adjustment range. This approach provides ultimate flexibility and user adjustment to tailor the product to the end application and supports fast turnaround delivery of products configured to exact user requirements, from stock held in several XP Power locations worldwide.

The architecture of the supplies uses a three-stage switching layout. The universal AC/DC front end has a bridgeless, interleaved power-factor-correction input that uses 65kHz switching. The primary switching, LLP resonant stage runs at around 120 kHz and employs a single, planar isolation transformer. Rather than rectifying the transformer output to a single intermediate bus, the secondary windings of the isolation transformer are available to each output module, and plug-in selection connects the secondary taps appropriate to the individual output selected. Each output module carries out synchronous rectification of the isolation transformer feed, followed by a 250-kHz switching buck or boost conversion to the final output. XP chose to offer a four-output format as its research indicated that the great majority of typical applications require three or four rails.

Complete article, here

AMP power group adds 60A PoL DC/DC to 2nd-sourced range

Architects of Modern Power – AMP – is a co-operative grouping of CUI, Ericsson Power Modules and Murata, who work together to offer *de-facto* “standard” formats of commonly required power conversion products, with the aim that a customer should always be able to find a true fit/form/function second-source for a range of units.

The alliance has now added a specification for a non-isolated digital point-of-load standard for 60 A output DC/DC converter; joining previously-released non-isolated DC/DC specifications, this one is called ‘gigaAMP’.

The standard sets out a mechanical and electrical specification; the AMP group, as part of its operation, promises that at least two of the three companies will produce independently-manufactured product conforming to the specification. The manufacturing path is second-sourced; the range does involve exchange of design information between the participating companies, in order to ensure fully-compatible operation in all aspects of a power module offering advanced power conversion technology for distributed power systems.

The ‘gigaAMP’ standard, introduced to provide a higher current option in a land-grid array (LGA) footprint, builds on the previously-released 'picoAMP' standard, published in September 2015, which defined standards for a lower range of non-isolated platforms ranging from 6A to 18A. The 60A 'gigaAMP' standard defines a compact footprint of 25.1 x 14.1 mm in an LGA format. As with other specification offered by the group, the converters will have fully matching features sets, and compatible configuration files and formats. This will allow a second-source product to be 'dropped in' to a production run, including where configuration is by digital download at final test stage, without disruption.

Complete article, here

Bluetooth Low Energy SoC steps up integration, flexibility

Dialog Semiconductor's claims for its SmartBond DA14681 include highest performance, lowest power consumption, smallest footprint and lowest system cost for creation of IoT devices, spanning wearables, smart home and other emerging IoT concepts.

The DA14681, Dialog says, intelligently balances performance and power efficiency, delivering high-power processing when it's needed - up to 96 MHz from its ARM Cortex M0 processor - and saving power when it isn't, by consuming less than 1 μA when in standby. This suits it for managing multi-sensor arrays and enables always-on sensing.

It supports the latest Bluetooth 4.2 standard, and its integrated Power Management Unit (PMU) provides three independent power rails to supply external system components, in addition to an on-chip charger and fuel gauge, allowing DA14681 to recharge batteries over a USB interface. Due to its unique architecture, it is able to power a complete IoT system without the need for additional external power management circuitry.

See also; Bluetooth SIG's developer toolkits address security, interoperability issues

Complete article, here

DESIGNING A DOHERTY AMPLIFIER FOR BROADCAST APPLICATIONS

By Peter Forth and Bill Goumas, Ampleon

Meeting technical requirements while under commercial pressure is as challenging today as it has always been, but by combining old techniques with new technology, it is possible to meet and even exceed these demands.

In its truest sense, the word broadcasting describes transmitting a signal across a wide area. In terms of radio and TV, broadcasting normally implies that the signal in question can be received by all of the subscribers in a given area at a level that will guarantee the quality of the content being transmitted.

Analogue services have the relative luxury of suffering signal degradation in a graceful way; a poor signal can still be heard or seen. But as digital transmissions continue to displace analogue services, the challenges in meeting subscriber expectations increase, as that same luxury of graceful degradation is not afforded to the encoding schemes used by digital services.

While a cellular service may have the benefit of a relatively dense network of basestations, terrestrial TV and radio transmitters are, quite literally, fewer and further between. Ensuring signal quality for these services is driving demand for more amplifiers that can offer both higher output power and greater efficiency. The question is; can semiconductor providers meet this growing demand and, if so, how will it be achieved?

Changing biases

Broadcasting digital TV is power-hungry. Today, the UHF amplifiers used for transmission are normally wideband power amplifiers configured in a push-pull output stage biased as Class AB. Biasing in this way is a recognised method for reducing crossover distortion in a push-pull configuration, but as both output transistor stages are conducting around the crossover point it does incur greater power dissipation which is contrary to the objective of power efficiency.

Another issue with this type of biasing is that amplifier average efficiency is relatively low; in the range of 25%. In an output stage in this application space, the power levels needed can easily reach 30 kW, so low efficiency directly translates to higher operating costs – simply in terms of the utility bill. Again, this is contrary to the desired result.

Because of this, the broadcast industry is intent on finding a solution that offers greater power efficiency in both respects; higher output efficiency and lower operating costs. The overriding requirement for any solution to meet these demands over a wide bandwidth does, of course, complicate things. But there are alternatives available.

Several methods are being aggressively pursued at the moment, which include Envelope Tracking (ET) and Envelope Elimination and Restoration (ERR), but while their use in wireless networks is now established, when applying these techniques in broadcasting, where the output power is significantly higher, they become less attractive in terms of their cost and complexity versus the benefits.

A further technique is available, one that is also proven and widely used in cellular networks, which does offer real benefits; the Doherty amplifier. Essentially, this combines a Class AB amplifier with a Class C stage (also known as a peaking stage), which extends the output power while minimising the level of distortion that would occur if Class AB amplification alone were used.

Despite being first developed in the 1930s, the eponymously named Doherty amplifier is as relevant today as it was over 80 years ago, in fact it could be said that the migration to digital transmissions makes it more relevant today.

There is, however, one challenge to be addressed; high power Doherty amplifiers are not traditionally considered to be wideband amplifiers. Indeed, they typically exhibit 10% or less fractional bandwidth, so the challenge now becomes adapting a Doherty amplifier design for use in an ultra-wideband application such as digital broadcasting.

Fractional bandwidth

In order to be applicable to broadcast, a Doherty amplifier would need to exhibit in excess of 30% fractional bandwidth, at the sort of output power needed for digital transmissions. *[Fractional bandwidth is the ratio of the difference between the upper and lower frequencies over which the amplifier operates – its bandwidth – to the centre frequency within that band. An amplifier with a usable range of 850 MHz to 1150 MHz would have a fractional bandwidth of 300/1000 (MHz), or 30%.]* In addition, the solution needs to be commercially viable, which effectively excludes the use of less standard materials, or more esoteric semiconductor fabrication techniques. And ideally the solution would also offer scaleability to higher output power levels.

It has been shown that it is possible to increase the bandwidth of a Doherty power amplifier by compensating for the output capacitance of the power amplifier and changing the configuration of the power combiner (peaking stage) and impedance transformation functions.

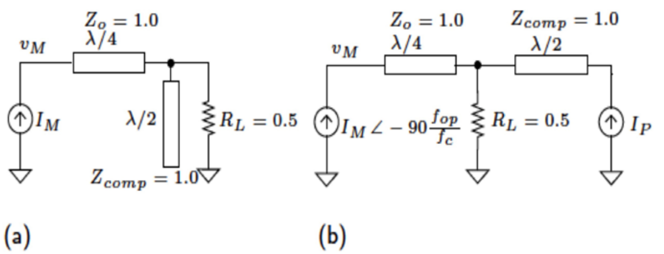


Figure 1a. *Wideband impedance inverter;*
Figure 1b. *Wideband Doherty power amplifier*

But this means the bandwidth is limited to that of the impedance inverter, which is typically a quarter-wave (λ/4) impedance transformer (QWTL), resulting in a bandwidth less than the target of >30% fractional bandwidth.

Research has shown that by adding an open circuit half-wave (λ/2) line to the load end of the impedance inverter, and before the peaking stage (Figure 1), it is possible to achieve a fractional RF bandwidth of more than 50%. Furthermore, the λ/2 line results in a wider load modulation bandwidth, giving an efficiency bandwidth in excess of 60%. Importantly, the peaking device can be placed at the open end of the λ/2 line without any effect on the back-off power level.

With the right design, the Doherty amplifier exhibits no bandwidth restrictions, even under full power. The results of the research carried out were encouraging enough to warrant further work into realising the potential of this initial work. Ampleon set about working on a detailed design based on its BLF888D, a 600W UHF LDMOS transistor (Figure 2). This device was chosen because it offers high bandwidth and high power output.

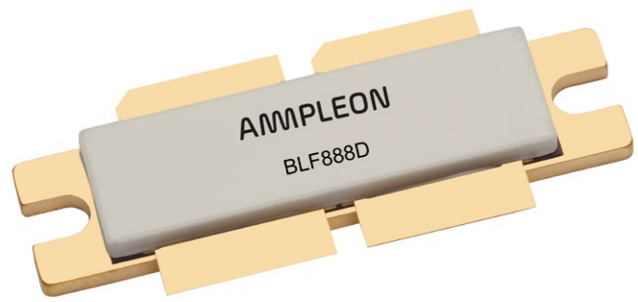


Figure 2. *BLF888D LDMOS transistor from Ampleon*

This article concludes by describing the impedance matching approach that has enabled a Doherty design with the required characteristics – click for pdf.

Download PDF of Article

Find RF PA Design on EETsearch

DATA ARCHITECTURE IN IOT: IDENTIFYING AND BREAKING DOWN SILOS

BY JAMES NOLAN

The Internet of Things (IoT) will generate unprecedented amounts of data—a staggering 400 zettabytes (ZB) of data a year by 2018, according to a report from Cisco. A major part of the value in this data will be in using it effectively across the enterprise or even across different enterprises and industries. If your legacy systems and/or new IoT data exist in silos, your IoT deployments will be limited in their ability to add value to the enterprise.

Before we can discuss the specifics of why silos are not ideal, it's important to discuss the nature of IoT data. Most different types of IoT deployments will generate different types of data. Some deployments will generate very high volumes of data that could be lots of noise and very little signal; let's take the transport sector for example. Highway traffic monitoring systems produce high volumes of video, but its value—to monitor traffic patterns—may not be that high; in other words, it may not detect any traffic jams or back-ups at all although massive videos have been produced. Other deployments will generate a much lower volume of data, which could be of very high value; for example, an emergency service generates data only when it detects a critical emergency event alarm that requires immediate action. In either example, messages may be flowing in both directions as well—such as a settings adjustment, a control message, or a configuration protocol message.

Even though you're likely going to be doing more than just collecting your data, you'll need to develop sophisticated data collection and management tools to extract value from it. You may find that you'll need data analytics or business intelligence tools to extract valuable information from the data in enterprise deployments.

In many cases, legacy enterprise IT infrastructure will form the basis for initial IoT deployments. For example, a recent survey from the Telecommunications Industry Association, and commissioned by my company InterDigital, found that 76% of companies are either exclusively or primarily focusing on integrating legacy business systems with IoT solutions to get them fit for purpose. Anyone with a passing familiarity of enterprise IT infrastructure will be able to see how the tendency exists for data to become silo-ed in legacy applications within an architecture that is not shared or available to other tools or applications. Some of the silos are formed due to different business organizations within an enterprise, but some of them are due to a non-scalable architecture. A typical design would call for one type of device to be connected via a secure gateway to a device management platform, and from there to a series of specific data services. That's a perfectly acceptable model for a small-scale deployment, but what if you wish to evolve and add a second type of device to your infrastructure? Or a third? Will the new devices be able to connect to the same type of gateway? Maybe. But can they also use the same data management platform and data services? If they can't, then silos form and your data will have limited use.

There are a number of different ways to get data out of silos. One approach is to look at how cloud-based data services can be integrated with your enterprise IoT deployments in a more open way than the one-to-one model described above. An example would be to almost think of putting all of your data in a marketplace or a "clearing house" type of public or private cloud solution, where it can be jointly used by many different data services at once. This helps improve efficiency in obvious ways, mostly by avoiding the duplication of data streams. But, in other ways, it liberates potential of data from one part of your deployment to be used by applications from another. That simple shift in thinking turns something that wasn't possible in the earlier example into a tangible solution.

Also see:

- Should your company build or buy its IoT infrastructure?
- Building the IoT: standards and hardware needs
- IoT has not yet lived up to the hype
- Discussion of the IoT must stratify

TRIMMING A DIGITAL-TO-ANALOGUE CONVERTER TO IMPROVE ACCURACY

By Rahul Prakash and Kunal Gandhi, Texas Instruments

More and more of today's modern industrial systems are requiring high accuracy. Traditionally, the test and measurement market has been the primary driver of highly accurate signal chain components, but now this trend is seeping into other markets such as factory automation, optical networking, and medical. Applications such as automated test equipment (ATEs), data acquisition cards (DAQs), and high-performance oscilloscopes require the highest accuracy signal chain.

Precision digital-to-analogue converters (DAC) are an integral part of the signal chain and are the primary facilitator of highly accurate signals. The precision DAC is typically used to fine-tune gain and offset, and minimizes other non-linearity. Therefore, it becomes the precision DAC that makes a signal precise as the DAC calibrates the signal. In this article, we talk about two different DAC architectures: R2R ladder and string DACs. Further, we analyze techniques that can help to enhance accuracy in both architectures.

Accuracy in precision DACs

There are many non-idealities associated with any analogue integrated circuit, and preci-

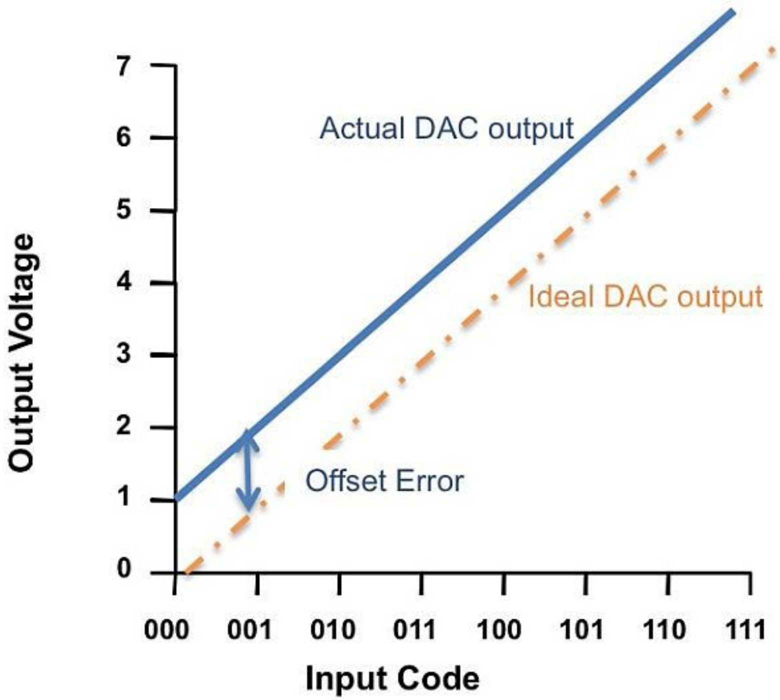


Figure 1. *DAC offset error of a simple 3-bit DAC.*

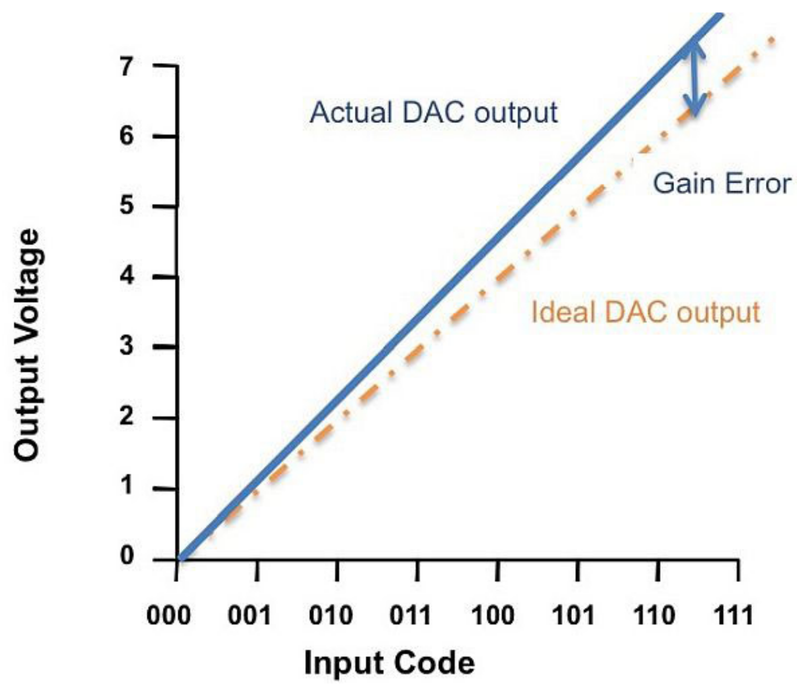


Figure 2. *DAC gain error of a simple 3-bit DAC.*

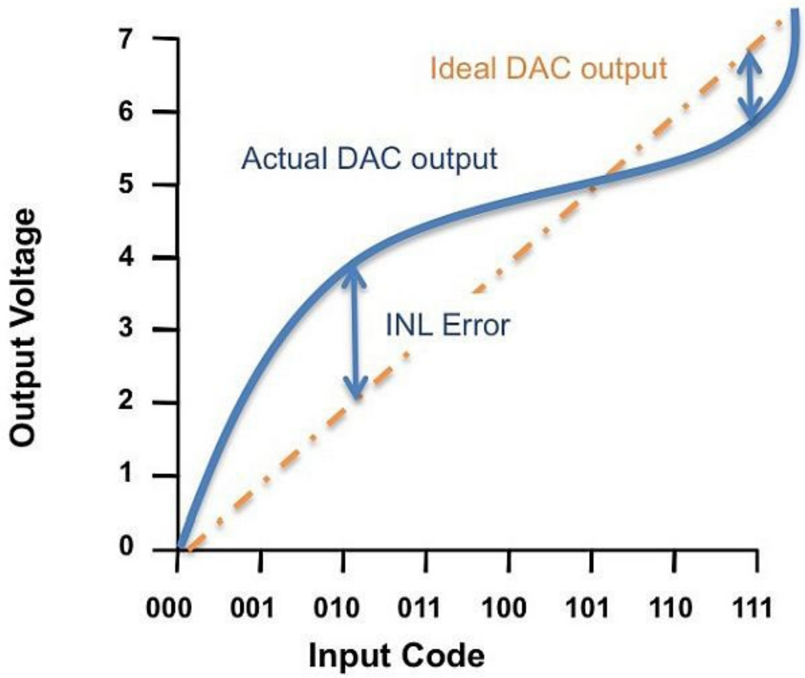


Figure 3. *DAC integral non-linearity of a simple 3-bit DAC.*

sion DACs are no different. The main source of direct-current (DC) errors in a precision DAC are offset error (OE), gain (GE), and integral non-linearity (INL). Offset error describes an offset or shift in the entire transfer function across the linear region of operation (Figure 1). Gain error describes the deviation from the ideal slope of the transfer function defined as a least significant bit (1 LSB), as shown in Figure 2. INL describes the deviation between the ideal output of a DAC and the actual output of a DAC. For example, Figure 3 shows an actual DAC output and an ideal DAC output for a simple 3-bit DAC.

A measure of a DAC's accuracy must include all three errors. The term total unadjusted error (TUE) is often used to quantify DAC accuracy. TUE is the root sum square (RSS) of these errors, equation (1), as these errors are uncorrelated.

The offset and gain errors are often calibrated on the system using a simple calibration scheme. The INL error, on the other hand, requires an extensive calibration scheme that involves many codes. This is a significant burden on the software and requires more memory bits (to store coefficients). Therefore, minimizing the DAC's INL is the key to enhancing accuracy.

INL in DAC architectures

The most common DAC architectures are R string- or R2R ladder-based topologies. The biggest contributor to INL for these DACs is mismatches in resistors used in ladder and string formats. Many analogue processes include a high-precision resistor to design ladders and string. As the demand for higher accuracy keeps increasing, having a high-precision resistor is insufficient. To address this concern, additional design, layout, and trimming techniques are being employed to counter the effect of these mismatches in resistors. This is where choosing either an R2R ladder or R string architecture plays an important role in the DAC's overall accuracy.

This article continues with a closer examination of both the R string and R2R ladder architectures, with a rationale for selecting according to the needs of an application for accuracy. Click for pdf.

Download PDF of Article

Find DACs on EETsearch

RED – NEW RADIO EQUIPMENT DIRECTIVE FOR EUROPE

BY HEINZ MELLEIN, ROHDE & SCHWARZ

Europe's new radio equipment directive (RED) has been effective from mid-June 2016 onward. The directive also covers radio receivers; they will have to meet minimum performance requirements in terms of sensitivity and selectivity.

Radio transmissions only with permission

Whoever wants to transmit or receive radio signals in Europe must comply with the relevant European directives governing the approval of radio equipment. These directives are developed in close cooperation between the European Commission, as a body taking an active part in political decision-making, and the European Electronic Communications Committee (ECC) within the European Conference of Postal and Telecommunications Administrations (CEPT), both of them guardians of the ever more valuable frequency resources; as well as the European Telecommunications Standards Institute (ETSI, Fig. 1).

Figure 1. *Regulatory bodies governing radio operation in Europe*

In addition to general requirements relating, for example, to the protection of health and safety or environmental compatibility, the directives also contain fundamental technical requirements. All radio equipment must fulfil what is referred to as "essential requirements" in the applicable directives, during normal operation and under the operating conditions specified by the manufacturer (ambient temperature, humidity, etc.). Evidence of compliance must be furnished by the radio equipment manufacturer or operator as a prerequisite for obtaining approval for operating the equipment and putting it on the market. To this end, the manufacturer or operator must submit a test report that has been issued by a certified test laboratory using validated measuring equipment, for example from Rohde & Schwarz.

Technical details on the diverse radio applications and frequency bands falling under the directives are specified in the "harmonized standards" developed by ETSI, along with possible test methods to demonstrate compliance. Harmonized standards become effective as European standards (EN) following a thorough examination by the regulatory bodies. Table 1 presents important examples of these standards. The currently applicable European standards are listed in the Official Journal of the European Union. An overview can be found on the ETSI website (www.etsi.org).

European standard	Equipment and frequency ranges covered by the standard	Test solution
EN 302 571	Intelligent transport systems (ITS), e.g. modules for car-to-car communications 5855 MHz to 5925 MHz	R&S TS-ITS100 RF conformance test system
EN 300 328	Wideband transmission systems, e.g. WLAN modules 2400 MHz to 2483.5 MHz (ISM band)	R&S TS8997 regulatory test system for wireless devices
EN 301 893	5 GHz high performance RLAN, e.g. WLAN modules 5.15 GHz to 5.35 GHz and 5.47 GHz to 5.725 GHz	R&S TS8997 regulatory test system for wireless devices
EN 301 908-13	IMT cellular networks, e.g. LTE user equipment E-UTRA frequency bands 1, 3, 7, 8, 20, 33, 34, 38, 40, 42, 43	R&S TS8980 RF test system family
EN 303 340	Digital terrestrial TV broadcast receivers; harmonized standard covering the essential requirements of article 3.2 of Directive 2014/53/EU	R&S BTC broadcast test center

Table 1. *Important examples of radio standards defining the technical details for compliance with the RED.*

The new directive also covers receivers; according to the Official Journal of the European Union L 153/62 of May 22, 2014, the previous directive RTTED-1999/5/EC, better known as R&TTE, has been replaced by the new radio equipment directive RED 2014/53/EU published on April 16, 2014. Replacement took effect on June 13, 2016, with an additional transition period of one year, subject to approval by the national legislative and regulatory bodies.

Technical aspects are essentially covered by Article 3.2, both in the previous and the new directive. In the previous directive, this article stipulated that a radio should only use the allowed frequency bands while avoiding interference with other bands. To fulfil these requirements, the transmitter section of a radio had to meet specified technical standards. Radio receiver sections and mere radio receivers (RX-only products) had always been exempt from the regulation.

The new RED adds an inconspicuous but crucial requirement to Article 3.2. Radios must make efficient use of the available spectrum. This is a consequence of the growing economic importance of radio resources. The directive now explicitly covers the receiver sections of radio equipment as well as mere radio receivers, and requires that they achieve a minimum level of performance in terms of sensitivity and selectivity, which must be demonstrated by appropriate measurements.
ETSI Recommendation EG 201 399 lists the typical radio transmitter and receiver parameters to be tested. A selection of these parameters includes, for transmitters – in line with previous (R&TTE) and new (RED) directives - Frequency accuracy and stability; Transmit power; Adjacent-channel power; Spurious emissions; Intermodulation attenuation; Transient behaviour; Modulation accuracy; and Duty cycle.
Parameters for receivers include, in line with the new directive (RED); Dynamic range and sensitivity; Co-channel rejection; Adjacent-channel selectivity; Spurious response rejection; Intermodulation response rejection; Blocking/desensitization; Spurious emissions; and Multipath sensitivity.

Summary

The new European radio equipment directive raises the demands on radio equipment of all types, calling for higher spectral efficiency. This means that from mid-2016, radio receivers will also have to meet regulatory minimum performance requirements, and consequently will have to be tested.

References

1. Directive 1999/5/EC of the European Parliament and of the Council, Official Journal of the European Union L 91/10 of April 7, 1999.
2. Directive 2014/53/EU of the European Parliament and of the Council, Official Journal of the European Union L 153/62 of May 22, 2015.

HOW TO EXTEND THE OPERATING TEMPERATURE OF FPGAS

By Arnaud Darmont, Aphesa

Some applications require electronics to operate at elevated temperatures, beyond the specified maximum operating junction temperature of the device. We will demonstrate that there are solutions to extend the operating temperature beyond the qualified maximum temperature, using as an example a design that was configured for the oil and gas industry; an oil well camera design.

The lifetime of any electronic device depends on its operating temperature. At elevated temperatures, devices age faster and their lifetime is reduced. Yet some applications require the electronics to operate beyond the specified maximum operating junction temperature of the device. An example from the oil-and-gas industry illustrates the problem and ways to solve it.

A customer asked our team at Aphesa to design a high-temperature camera that will operate inside oil wells (Figure 1). The device required a rather large FPGA and had temperature requirements up to at least 125C—the system's operating temperature. As a consultancy that develops custom cameras and custom electronics including FPGA code and embedded software, we have experience with high-temperature operation. But for this project, we had to go the extra mile.

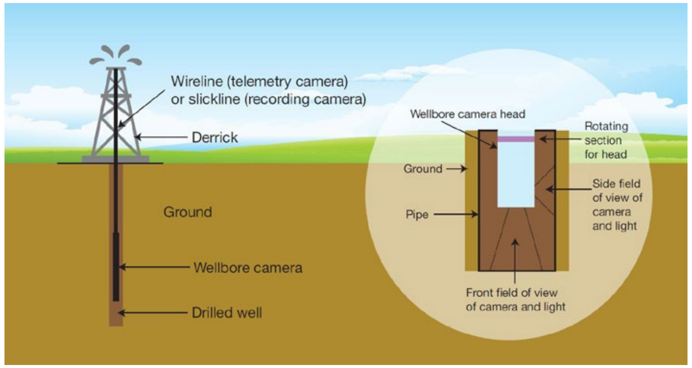


Figure 1. *The design of a high-temperature camera to operate inside oil wells required extending the operating temperature beyond the qualified maximum temperature of the device.*

The product is a down-hole, dual, colour camera designed for use in oil well inspection (Figure 2). It performs embedded image processing, colour reconstruction and communication. The system has memory, LED drivers and a high-dynamic-range (HDR) imaging capability. For this project we chose to use the XA6SLX45 device from Xilinx (Spartan-6 LX45 automotive) because of its wide temperature range, robustness, small package, large embedded memory and large cell count.

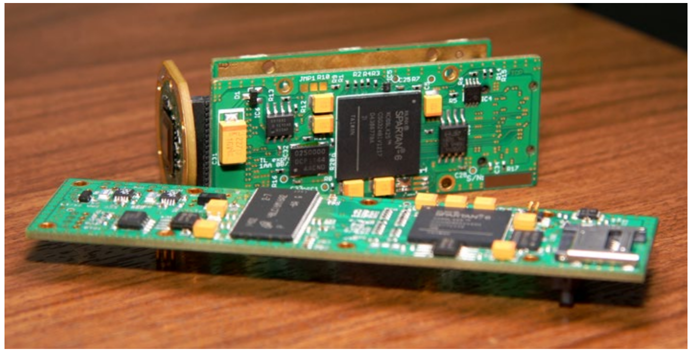


Figure 2. *The high-temperature camera and high-temperature processing board are equipped with Xilinx Spartan-6 FPGAs.*

This project was quite challenging also lots of fun to do. Let's take a look at how we put it all together, starting with a review of some concepts of temperature, including junction temperature, thermal resistance and other phenomena. We will look into the causes of temperature increase in a device and will list our solutions to prevent it. We will also address the possible hot-spot issues and propose solutions to them.

In this particular project, the use of thermoelectric cooling was limited and we had to find other solutions.

Temperature variation

Electronic devices are usually specified with their maximum junction temperature. Unfortunately, what the system designers are concerned with is the ambient temperature. The difference between the ambient and the junction temperature will depend on the capability of the package to transfer heat and the cooling system to dissipate this heat outside of the system's enclosure.

Thermal resistance is a heat property and a measurement of how much a given material resists heat flow. Heat generated in the active die of a device meets this resistance as it flows to ambient, and the die is therefore at a higher temperature than ambient.

$$T_j = T_a + (R_{th,\ package} + R_{th,\ ambient}) \ .\ P$$

Equation 1. Relationship between ambient and junction temperatures where T_j is the junction temperature, T_a is the ambient temperature, $R_{th,\ package}$ is the thermal resistance between the junction and the outside surface of the package, $R_{th,\ ambient}$ is the thermal resistance between the outside surface of the package and the ambient air (it is zero if there is no heat sink or air flow) and P is the power dissipated by the device.

The energy dissipated as heat depends on the device, the circuit, the clock frequency and the code running in the device. The temperature difference between the inside of the device (the junction temperature) and its environment (the ambient temperature) therefore depends on the device, the code and the schematic.

Usual cooling solutions

In most designs where cooling is required, designers use either passive cooling (a heat sink that helps dissipate heat into the air by increasing the surface area in contact with air) or active cooling. Active-cooling solutions typically force an airflow in order to help renew the cold air that absorbs heat above the device. The capability of air to absorb heat depends on the temperature difference between the air and the device, as well as on the pressure of the air. Other solutions include liquid cooling, where the liquid, usually water, replaces air for more efficiency. The capability of a mass of air or fluid to absorb heat is given by the heat absorption equation;

$$Q = mc\Delta T$$

Equation 2. Heat absorption equation, where Q is the maximum heat that can be absorbed, m is the mass of the heat-absorbing material, c is a constant representative of the material and ΔT is the difference between the ambient temperature of the heat-absorbing material at the beginning and the final temperature. This formula is valid for a nonrenewing heat-absorbing material and a net amount of heat to be absorbed, an unrealistic situation but which already shows that pressure (mass), type of material (c) and outside temperature play a role in the efficiency of cooling.

The final approach that designers often use is thermoelectric cooling, where the Peltier effect—a temperature difference created by applying a voltage between two electrodes connected to a sample of semiconductor material—is used to cool one side of a cooling plate while heating the other. Although this phenomenon helps to move heat away from the device to be cooled, Peltier cooling has one big disadvantage: it requires significant external power.

The article continues, outlining the steps taken by the design team to allow the FPGAs to operate at elevated temperatures without ill effects – click for pdf

Download PDF of Article

Find FPGAs on EETsearch

EMBEDDED SYSTEMS PERFORMANCE - GETTING MORE OUT OF YOUR MCU DURING DEBUG

By Johan Kraft, Percepio

Microcontrollers are becoming increasingly capable of handling advanced applications but unfortunately for developers, that also means debugging firmware has become increasingly complex. It may not be possible to call repeatedly on the simple 'printf' function to send debug information over a serial port, in a system where maintaining determined execution time is an inherent and important part of its operation.

In such systems, access to diagnostic information becomes more important, not less; the use of an invasive approach to debug is untenable. Fortunately, a solution may be available to many developers, specifically those using an ARM Cortex-M3, -M4 or -M7 based MCU.

Part of the ARM CoreSight debugger technology is the Serial Wire Viewer (SWV) real-time trace module, which includes the Instrumentation Trace Macrocell (ITM). This allows arbitrary data to be sent to a debugger as Software Instrumentation (SWIT) events, while the system continues to run at full speed. As Figure 1 shows, the ITM is closely linked to the Data Watchpoint and Trace (DWT) unit, and is connected to the trace port and debug port using the Serial Wire Out (SWO) interface.

The ITM generates data in packets, which can originate from multiple sources. If packets arrive from several sources at the same time, it arbitrates the order in which the packets are output. Highest in priority is the software trace; it allows software to write directly to ITM registers. Next in line are packets generated by the DWT, comprising four comparators that can be user-configured as a hardware watchpoint, an Embedded Trace Macrocell (ETM) trigger, a PC sampler event trigger, or a data address sampler event trigger. Timestamping is also supported, so each ITM or DWT packet may also produce a corresponding timestamp packet, which will have lower priority in the arbitration.

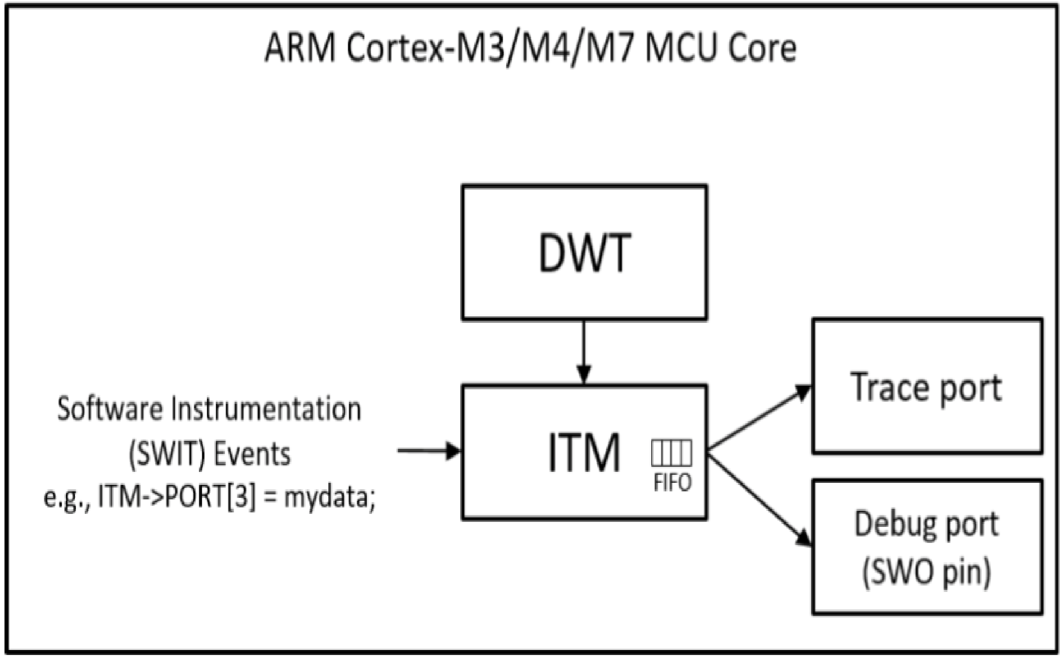


Figure 1. *Connectivity of the Instrumentation Trace Macrocell within a Cortex core*

Minimal overhead

By writing to an associated register, any kind of data can be sent to the host system as SWIT events using the ITM. Because this can be accomplished in a very small number of clock cycles, while supporting timestamping, it can provide invaluable insights into real-time processes. This powerful functionality can be

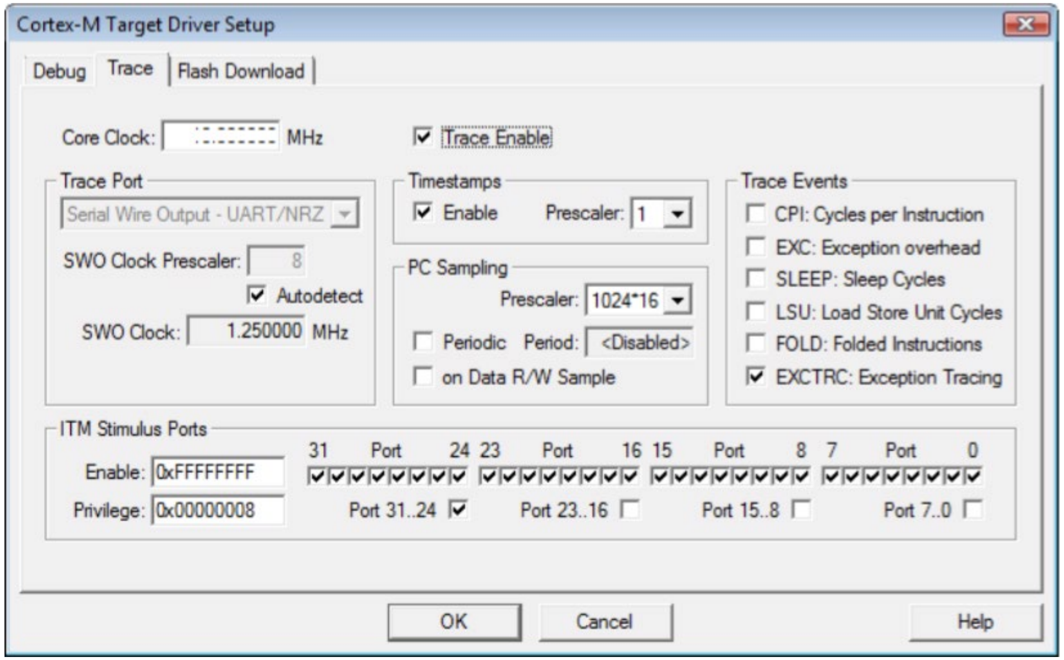


Figure 2. *The ITM as handled in the Keil µVision integrated development environment.*

```
#include <myboard.h> // Includes CMSIS
…
ITM->PORT[0] = mydata;
```

Figure 3a. *Instruction fragment for data writes.*

```
#define ITM_PORT(n)   (*((volatile unsigned long *)(0xE0000000+4*n)))
…
ITM_PORT(0) = mydata;
```

Figure 3b. *Instructions fragment to write to the ITM other than via CMSIS.*

accessed from within any IDE that supports ITM tracing. Once enabled, it is just a case of writing to the ITM stimulus registers, which are located at 0xE0000000 (port 0) to 0xE000007C (port 31). As an example, Figure 2 shows how to enable ITM in the Keil µVision IDE.

Once enabled, using the ITM is as simple as writing data to the right register. Figure 3a shows the instruction used to write data if the ARM CMSIS API is already supported in the Board Support Package (BSP) being used.

Even systems that aren't using the CMSIS API can use the ITM, the code required is shown in Figure 3b. It is possible to send 'printf' type text data this way, or simply send binary data; the ITM allows up to 32 bits per write.

As shown in the configuration screen (Figure 2), and outlined above, the ITM features 32 logic channels that can be used for SWIT events. Users are free to use these channels in any way they like, however ARM recommends using Channel 0 for text data and Channel 31 for RTOS events. This leaves a further 30 channels that could, for example, be assigned logically to pass specific types of debug data.

Another benefit of using the ITM is the ability to implement more advanced forms of software tracing, using the DWT. For instance, you can trace all accesses of a particular memory address, or use it to trigger detailed instruction trace (ETM) for a particular piece of code. Furthermore, the DWT contains counters for clock cycles, folded instructions, load-store unit operations, sleep cycles, CPI and interrupt overhead. It can also be configured to generate PC samples at defined intervals, as well as generating interrupt event information.

While extremely powerful and flexible, it is important to appreciate that all the ITM channels use a common 10-Byte FIFO buffer (refer to Figure 1), which feeds both output ports. If an advanced trace debugger is being used, the ITM data is included with the ETM, as well as the SWO interface. Most debug probes designed for the ARM Cortex-M family will support the SWO interface. As the FIFO buffer is relatively small, any debug probe used should be fast enough to avoid data losses; if a probe is too slow, data may be overwritten. One way to avoid this is to implement a FIFO check before writing to it, and delay the write if there is no space available.

Clearly, this will have an impact on system performance, so a better solution would be to use a fast debug probe. Many of the market leaders support very high SWO sampling rates (60 MHz or more), which should ensure no data loss at full speed. A recent exercise to test this theory, using a Keil ULINKpro, resulted in write speeds of more than 2 MByte/sec using the ITM. This is many times more than usually required, even for tracing all RTOS events with a tool such as Percepio Tracealyzer.

The test was conducted using a tight loop of optimised code running on an ARM Cortex-M4 based MCU at 168 MHz. Even at the highest possible execution speed, the data was received without error. It did result in some ITM blocking as the FIFO buffer sometimes got saturated; the average write time was 20 cycles and at most 100 cycles. But reducing the data rate to 1 MByte/sec resulted in no ITM blocking whatsoever. Each ITM write took just 7 clock cycles, so the impact on a real-time system would be effectively imperceptible.

Conclusion

By adding one line of code (Figure 3) to those points in application code where debug data is advantageous, developers get instant access to the inner machinations of their embedded software, allowing verification between intent and action. The ITM is included in all Cortex-M3, -M4 and -M7 MCUs today, and is likely to be improved in future MCUs. Many IDEs already support ITM and Percepio is working on adding support for ITM-based RTOS tracing in Tracealyzer in the near future.

This 'free' debug technology provides an invaluable insight into embedded code, and represents an evolution from the invasive 'printf' approach to debugging. It offers almost instant productivity gains for developers, while introducing little or no performance overheads.

Dr Johan Kraft is CEO and founder of Percepio

TRANSIMPEDANCE AMPLIFIER COMBATS VOLTAGE AND CURRENT NOISE

By Glen Brisebois, Linear Technology

Einstein published his seminal paper on the photoelectric effect 110 years ago, essentially inventing the discipline of photonics. One would think that over so many years the science and engineering surrounding photonics must have fully matured. But not so. Optical sensors—photodiodes, avalanche photodiodes, and photomultiplier tubes—continue to achieve astoundingly high dynamic ranges, enabling electronics to peer ever more deeply into the photonic world.
Photosensors typically convert photons to electron current and are followed by a transimpedance function to transform the current into a voltage. The transimpedance function may be either a simple resistor or,

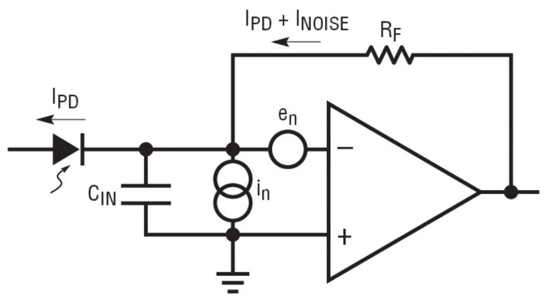


Figure 1. *The op amp with its noise sources and input capacitance (see pdf download for complete Figure 1).*

for higher bandwidth, the summing node of an op amp, in which case it is called a transimpedance amplifier (TIA). The traditional enemies of the TIA are voltage noise, current noise, input capacitance, bias current and finite bandwidth. Enter a new design with 4.25 nV/√Hz voltage noise, 0.005 pA/√Hz current noise, a very low 0.45 pF of input capacitance, 3 fA of bias current and 4 GHz of gain-bandwidth.

Understanding voltage & current noise contributions in TIAs

Output noise in TIAs is a result of combined input voltage noise and input current noise. This combined effect is often specified as a current noise referred to the input—essentially the output voltage noise divided by the gain in Ohms—but it actually arises from both input noise sources. In fact, the dominant cause of output noise is usually input voltage noise (Figure 1).
By virtue of feedback, the minus input is fixed at virtual ground so the current noise i_n passes directly through R_F and contributes to total current noise with a factor of 1. Also by virtue of feedback, the voltage noise e_n is placed in parallel with the input capacitance C_{IN} and induces a current noise of $e_n/Z(C_{IN})$. The impedance of a capacitor is 1/2πfC, so the effective current noise due to input voltage noise and capacitance is $2\pi fC_{IN}e_n$. So the total op amp noise (ignoring RF thermal noise) is

$$I_{NOISE} = \sqrt{(2\pi fC_{IN}e_n)^2 + (i_n)^2}$$

This is sometimes referred to as CV + I noise and makes an excellent figure of merit for an op amp, because it incorporates only op amp characteristics, neglecting external aspects of the circuit such as photosensor capacitance and R_F thermal noise. It is essentially the best the op amp can do.

This article continues with a detailed calculation of noise for different amplifiers; explores amplifier performance in low-noise amplifiers for photonic detectors; and discusses in depth the circuit construction and measurement techniques required for stable operation in the regime of TeraOhm resistors and femtoAmp resolution. Click for pdf.

Download PDF of Article

Find Photonics Amplifiers on EETsearch

THE EMERGING TRIANGULAR RELATIONSHIP OF MOBILE CONNECTIONS

By William Powell, Rohde & Schwarz

A characteristic feature of mobile communications is that subscribers operate in a network of base stations used to process all communications. Future mobile devices will additionally be able to exchange data without an intermediate base station if they are in close proximity to each other. A tester for this scenario must be able to simulate not only a base station but also a mobile device with corresponding functionality.

With the advent of device-to-device functionality (D2D) in Release 12 of the 3GPP specification, proximity services (ProSe) are possible for the first time in the history of cellular mobile communications. ProSe is based on a direct data transfer between two UEs (user equipment). The use of such services has to be authorized, i.e. covered by the subscriber's cell phone contract. Once this is in place, the need for the base station is eliminated and under certain circumstances the devices can be used like walkie-talkies. The motivation for D2D is twofold. The first is an emergency or major disaster situation. If the mobile network is unavailable due to a power failure or if the rescuees or rescuers do not have network coverage, for instance in a cellar, self-sufficient mobile devices are exceptionally helpful. The second application scenario relates to local broadcast services, namely unidirectional data transfer.

To be able to handle D2D, the mobile device (UE) must have the new LTE D2D interface, which is called a sidelink. The UE is expected to be able to communicate over distances up to 500m over the sidelink. D2D as per Release 12 can be implemented in two different forms: sidelink direct discovery (for broadcast) and sidelink direct communication (for groupcast). Both are possible in FDD as well as TDD networks and use the resources for the UL LTE Uu interface, which are allocated to the sidelink for this purpose. Direct communication is reserved for safety-related applications (see below for more detail), but the direct discovery feature is also open to commercial applications. In documentation from technology suppliers and

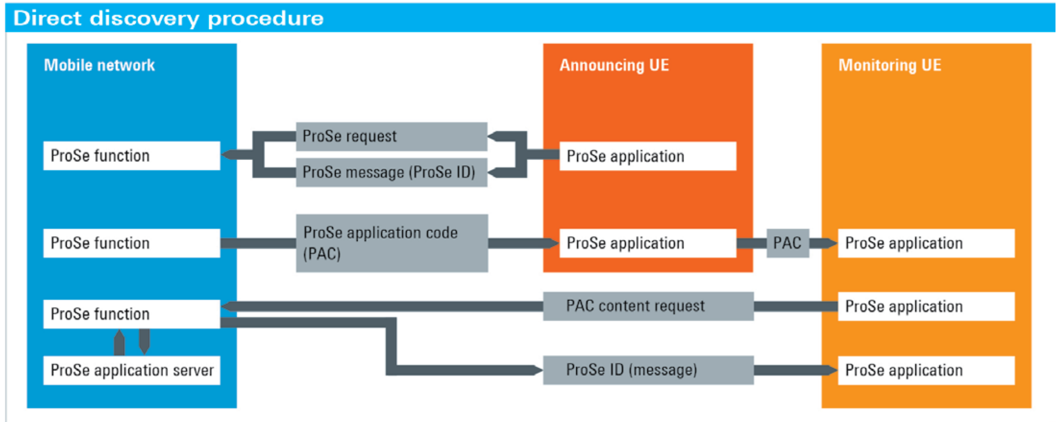


Figure 1. *Direct discovery means that a UE uses the network to broadcast locally relevant information to nearby receivers.*

network operators, this feature is referred to as LTE Direct (Qualcomm) and LTE Radar (T-Mobile).

No ProSe usage without authorization

Irrespective of whether the user would like to use the direct discovery or direct communication service, the UE first determines if it is authorized. If the UE has network coverage, this is usually done via a network request. The UE uses existing DNS lookup procedures to find the responsible server (ProSe function) at the contracting company. If there is no network coverage, a UE can be pre-provisioned for ProSe services by having ProSe authorization stored on the SIM card or in the UE file system. Rohde & Schwarz offers the R&S CMW-Z6 SIM card option to test this capability.

Direct discovery: efficient messaging with network support

Sidelink direct discovery is an extremely efficient method for broadcasting locally relevant information to other nearby receivers. For example, retail businesses can use this feature to advertise special promotions. The announcing UE periodically transmits the ProSe application code (PAC), a short 184-bit data telegram, over the sidelink air interface (see Fig. 1). The monitoring UE forwards the PAC to the network ProSe function, where it serves as an access key to the actual XML-based user information (ProSe ID). The ProSe function delivers this previously uploaded ProSe ID to the monitoring UE over the mobile network.

An announcing UE's ProSe application first requests a PAC, such as:

"mcc123.mnc456.ProSeApp.Theatre.Tickets.Sales.Available.2",

and forwards it together with the broadcast information to the provider. If the provider gives a green light (which depends on the current network load and other criteria), the mobile network operator (MNO) responds to the request by issuing a PAC that is intended for broadcasting.

The specific design of the whole process in actual networks has not yet been finalized. One of the open questions is how to ensure that the message reaches every LTE subscriber, even when the transmitter and receiver are operating on different frequencies or are registered with different providers. 3GPP does not specify how two MNOs allow access to each other's ProSe function. The technical principles, however, are established in Release 12 so that the basic process can be simulated. The R&S CMW500 with the Release 12 option can simulate this process.

The article continues with a further exploration of how the device-device modes will operate, and how they may be developed and tested – click for pdf.

Download PDF of Article

Find LTE Test on EETsearch

designideas

- Op amp makes precision clipper
- Circuit delivers constant power to a load

Op amp makes precision clipper

By Thomas Mosteller & Aaron Schultz, Linear Technology

It can be a challenge to match the voltage range of an analogue signal to the input range of an analogue-to-digital converter (ADC). Exceeding the ADC's input range will give an incorrect reading, and if the input goes far enough beyond the power supply rails, substrate currents can flow into the ADC, which can cause latch up or even damage to the part. However, restricting the input voltage range to lower, more conservative levels wastes the ADC's dynamic range and resolution.

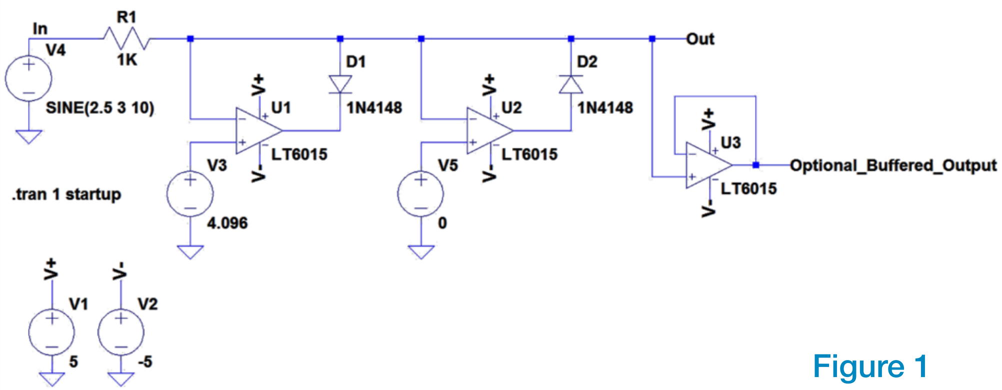


Figure 1

The simple op amp clipper shown in Figure 1 prevents these problems. The maximum allowable input voltage is applied to the non-inverting input of U1, and the output is fed back to the inverting input via small signal diode D1. The ADC's reference voltage can be used for the clipping reference if it's available. When the input voltage is below the reference, U1's output is driven to the positive rail and D1 is reversed biased, so the input signal passes through without being altered. When the input goes above the clamp voltage, the op amp output reverses and closes the loop through D1, effectively becoming a unity gain follower to the clamp voltage. The input resistor R1 limits the amount of current the op amp output has to sink. The second op amp U2 performs the complementary negative clipping function, preventing the signal from going below ground. Thus the output signal is restricted, to 4.096V to 0V out in this example.

While simple in concept, this circuit poses unique challenges for the op amp. First, most modern op amps have back-to-back diodes across the input to prevent the application of large differential voltages to the inputs which can cause damage to the part or shifts in the input offset voltage. In this circuit, these diodes would prevent the output signal from going more than one diode drop below the positive clamp voltage or one diode drop above the negative clamp voltage. Deciding whether a given op amp has these diodes can require some detective work. Some parts' data sheets show the presence of the input diodes, but others don't. Another indication of the diodes' presence is a limitation in the Absolute Maximum Ratings section of input current to a few mA.

In addition, the output of the op amp has to slew from the "unclamped" to the "clamped" state as quickly as possible in order to clamp a fast rising signal without a potentially dangerous overshoot. Furthermore, rail-to-rail input and output operation of the op amp is desired so it can function with voltages close to the limits of the power supplies.

The LT6015 family of op amps, which includes the LT6016 dual and LT6017 quad versions, address these issues. There are no diodes on the inputs so they are permitted to have a ±80V differential voltage, which should not impose a limitation on any practical ADC application. The input voltage can go as high as 80V above or 25V below the V- rail, which allows the part to survive inputs that would damage other parts.

The LT6015 is further unique in that it allows a power supply range from V+ to V- of up to 60V, which would allow use of the circuit to clamp higher voltages than the great majority of op amps. It also has a slew rate of 0.75 V/µsec, which allows it to clamp reasonably fast rising signals. The sub 100 µV typical offset voltage ensures that the clamping level is very accurate.

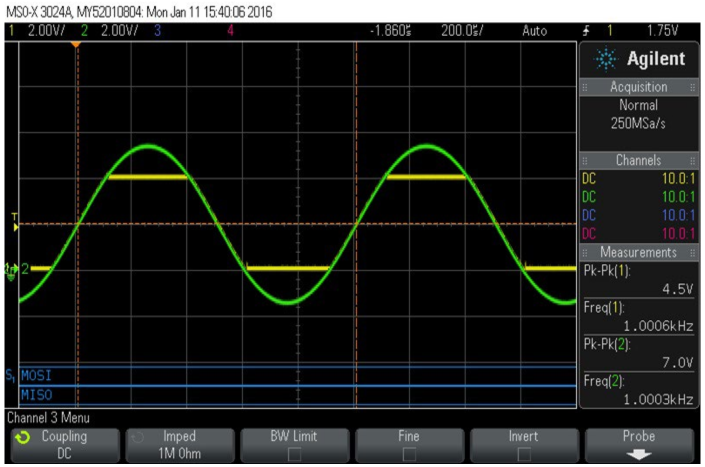


Figure 2.

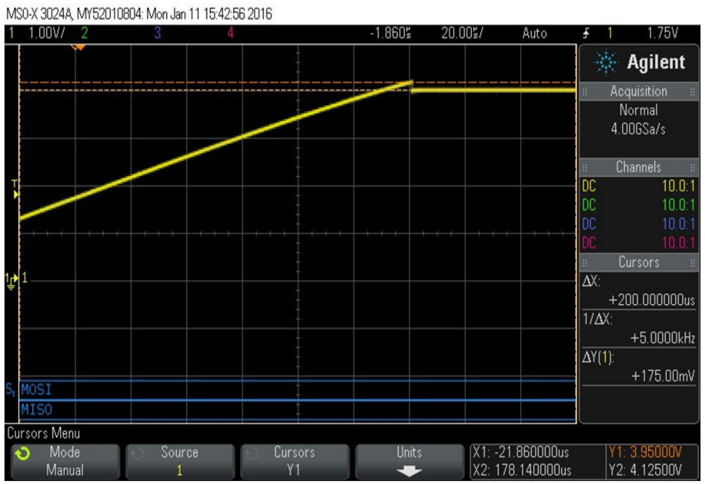


Figure 3.

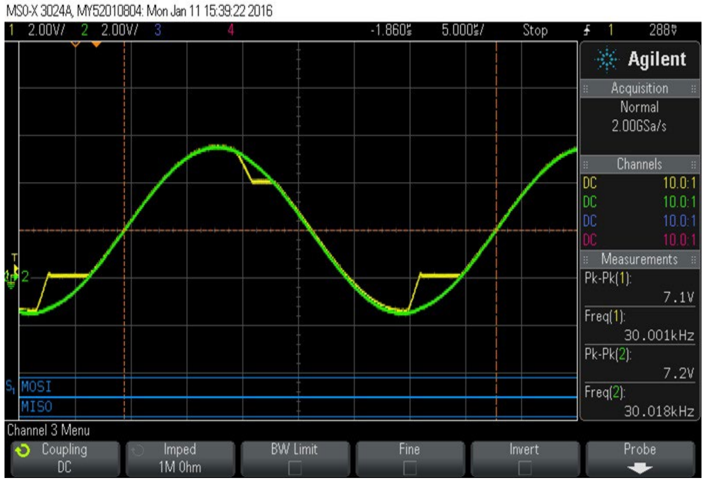


Figure 4.

Figure 2 shows the LT6105 driven from ±10V supplies clamping a 7V pk-pk 1 kHz sine wave at 0 and 4V. It's hard to see the clamping action, but if you zoom in on the output you can see a small overshoot in Figure 3. Increasing the input frequency to 30 kHz in Figure 4 clearly shows the clamping action taking place in less than 10 µsec, limiting the operating bandwidth of the circuit to a few kHz. The clamping speed can also be increased by limiting the voltage supply rails to close to the clamping limit voltages, which lowers the voltage range the output must slew to go into clamping mode. Since the LT6105 output swings very close to the supply rails, little extra voltage range is required.

Another limitation on this circuit is that the output resistance is defined by R1, which needs to be at least a few hundred Ohms in order to limit the output of current in the op amp output. Some ADCs need to be driven by a low resistance so buffer amp U3 might be required. The LT6017 quad package would permit a single part to perform all these functions.

***Thomas Mosteller** is a Field Applications Engineer, and **Aaron Schultz**, Applications Manager at Linear Technology.*

Circuit delivers constant power to a load

By Kiril Karagiozov

If you have a load with a variable or poorly specified resistance and want to regulate the power applied to it (a heater for example), merely controlling the voltage or current will not work, as in both cases the power $P = I^2R = V^2/R$ depends on R.

Instead, let us generate pulses with constant energy E_{pulse}, independent of the resistance of the load R_L. Then by changing the frequency f of the pulses we can conveniently and precisely control the load power ($P = f{\cdot}E_{pulse}$), from 0 to a known maximum level.

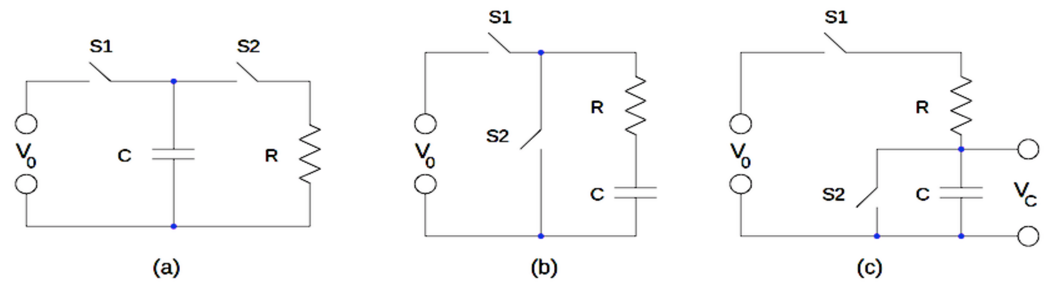


Figure 1. *Constant energy impulses*

Figure 1a shows a simple way to generate a constant energy pulse. Capacitor C is charged to an initial voltage V0, storing $½CV_0^2$ Joules. It is then discharged through the load. The pulse has a constant energy that does not depend on R_L.

Such a simple approach has drawbacks. First, it is wasteful. In order to charge the capacitor with $½CV_0^2$ joules, another $½CV_0^2$ joules are lost (see Appendix for details). The circuit of Figure 1b fixes that problem – all resistive losses now occur in the load.

One thing to note is that the power distribution of the pulse is quite uneven. About 63.2% of the energy is delivered in the first ½τ ($\tau = R_LC$; energy lost in the load evolves twice as fast as the voltage rises, hence the factor ½). It takes a further ½·4τ for the next 36.1% of energy, which is equivalent to only about 1/7 of the average power during the first ½τ. The uneven power distribution limits the maximum power that can be controlled by the circuit. It takes infinity to transfer the remaining 0.67% of the energy. In practice this will be ignored, limiting accuracy.
However, as shown in Figure 1c, we can interrupt charging after the capacitor has reached a certain threshold value, V_C. The energy dissipated in the load is equal to $CV_CV_0 - ½CV_C^2$ and is again independent of the value of R_L (see Appendix for derivation).

When choosing the value of V_C, the main consideration is overshoot, which causes the energy of the pulse to be higher than calculated. The slew rate at the moment the threshold is reached is equal to:

$$\frac{dV}{dt}=\frac{I}{C}=\frac{V_0-V_C}{R_L{\cdot}C}$$

A lower threshold value V_C results in higher overshoot for the same comparator speed.
The Design Idea in Figure 2 shows one possible implementation. A 555 provides switches, a comparator, and logic. The trigger input is biased above the trip point by divider R1 & R2. Triggering pulses pass through a small capacitor, C1 (2-10 pF), in order to prevent saturation of the comparator (see 8.3.1 of the datasheet). The maximum operating frequency is therefore comparable to that of an oscillator.

The R3-R4 divider sets the threshold voltage. A TL431 shunt regulator (see datasheet for the selection of R6-R8) sets the charge voltage. Depending on the chosen values, R5 (a couple of ohms) may be needed to prevent excessive current in the shunt regulator. The actual charge voltage will be higher by the forward voltage drop of D1. Use a fast diode for D1 and a film capacitor for C.

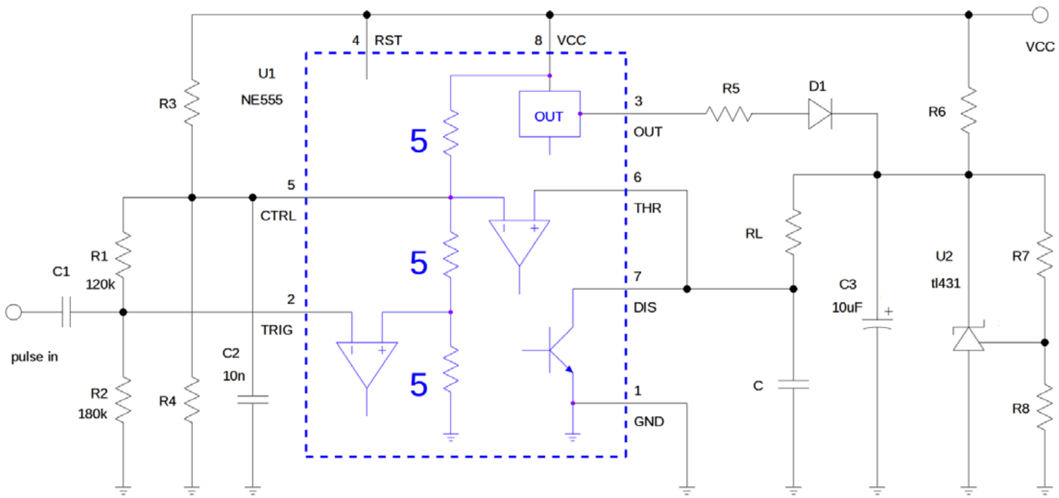


Figure 2. *Basic implementation of the constant power circuit*

With a more elaborate control circuit, the wasteful discharge to ground can be eliminated. For example, capacitor C can be made to charge from -V/2 to +V/2 through R_L from a positive rail V_0-V/2 and discharge through RL to a negative rail $-V_0$+V/2, creating a symmetrical pulse for both charge and discharge, and no wasted energy. Alternatively, the voltage of the capacitor can be made to oscillate around a midpoint above ground.

This design was used to construct a power supply for a thermally driven MEMS.

Appendix

Figure 3 shows a circuit where a capacitor is charged from a potential V_0 to a potential V_C. Charges moving from a higher to a lower potential perform work W = qΔV.

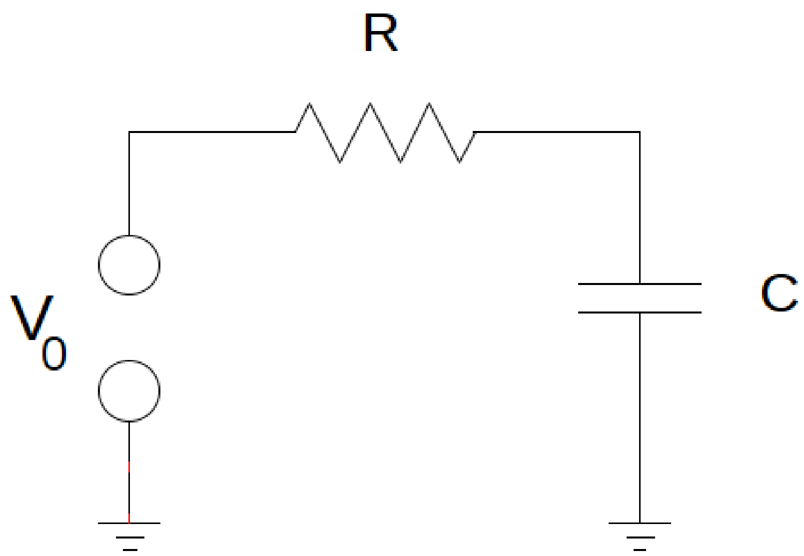


Figure 3. *Charging a capacitor*

Charge is discrete, so we can look at the contribution of each individual charge. Such a charge starts from a state of rest at potential V_0 at the source and ends up at rest on the plate of the capacitor at a certain lower potential V_C.

If capacitor C is completely discharged initially, the work done by each charge follows the pattern:

$$W_0 = q\left(V_0 - \frac{0\cdot q}{C}\right)$$

$$W_1 = q\left(V_0 - \frac{1\cdot q}{C}\right)$$

$$\vdots$$

$$W_n = q\left(V_0 - \frac{n\cdot q}{C}\right)$$

Here, n·q is the total charge Q on the capacitor after n individual charges, and;

$$\frac{n\cdot q}{C} = \frac{Q}{C} = V_C$$

is the voltage to which the capacitor is charged. From that relationship we determine the number of charges,

$$n = \frac{V_C\cdot C}{q}$$

The total work is equal to the sum of the contributions of each charge: W = $W_0+W_1+\ldots+W_n$. Expressed as a function of V_C, the work $W(V_C)$ is then equal to:

$$W(V_C) = \sum_{n=0}^{n=\frac{V_C\cdot C}{q}} q\left(V_0 - \frac{n\cdot q}{C}\right)$$

Simplifying, we obtain:

$$W(V_C) = \sum_{n=0}^{n=\frac{V_C\cdot C}{q}} qV_0 - \sum_{n=0}^{n=\frac{V_C\cdot C}{q}} \frac{n\cdot q^2}{C}$$

$$\approx \frac{V_C\cdot C}{q} qV_0 - \frac{q^2}{C} \sum_{n=0}^{n=\frac{V_C\cdot C}{q}} n$$

$$\approx C V_C V_0 - \frac{q^2}{C}\cdot\frac{1}{2}\frac{V_C^2 C^2}{q^2}$$

$$= C V_C V_0 - \frac{1}{2} C V_C^2$$

The first part stands for the energy taken from the voltage source. The second part is the energy which the capacitor holds when charged to a voltage V_C. The difference is the energy lost, converted to heat in the load. As the equation shows, it does not depend on R in any way.

If we charge the capacitor to the full potential of the source, V_C equals V_0. The source then supplies CV_0^2 joules, the capacitor holds ½CV_0^2 joules, and another ½CV_0^2 joules are converted to heat.

***Kiril Karagiozov** is driven to make useful things that work. As these usually have some sort of electronics in them, he gets to rekindle his childhood fascination with circuits.*

productroundup

productroundup

Altium's CircuitStudio, as a distribution download

Distributor Farnell element14, in partnership with Altium, has released version 1.2 of Altium CircuitStudio; the package is a full professional PCB design tool with schematic capture, feature-rich PCB editing and centralised component management. It is now available at a price point of €957 / £753. Altium CircuitStudio is a complete PCB design system with a balanced blend of powerful features that include; Design Rule Driven Interactive Routing enables designers to quickly and efficiently route without worrying about breaking any preset design rules; Built-In Autorouter Engine provides the routes from one pin to another automatically based on predetermined rules set by the designer; Native 3D PCB Visualization Engine allows designers to ensure their boards fit their mechanical enclosures the first time, effectively reducing design spins and saving time and resources.

Complete article, here

Intel Curie module for wearable & edge devices

Distributor Mouser Electronics has the Intel Curie module (Intel's "computer on a button"), a complete low-power solution designed for use in wearable devices and consumer and industrial edge solutions. Hosting a Quark SE SoC, the Curie module is power efficient and offers features for "always-on" applications such as social media, sports, and fitness activities. Alongside the 32-bit Quark SE SoC is 384 kBytes of flash memory and 80 kBytes of SRAM. The module includes an integrated DSP sensor hub, a 6-axis combination sensor with accelerometer and gyroscope, and Bluetooth low energy.

Complete article, here

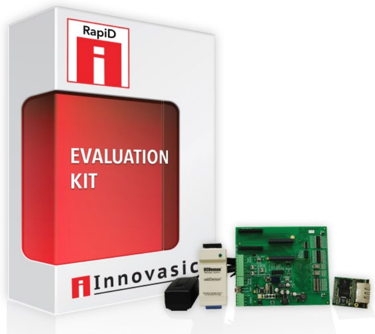
Chip-scale atomic clocks extend temperature ranges

With full operating and storage temperature, these Microsemi devices are aimed at high-reliability applications in defence, underwater geophysical survey and scientific markets. The thermally improved Chip Scale Atomic Clock (CSAC) components offer the lowest power holdover atomic clock technology. With an operating temperature range of -10 to 70C the components feature 17 cm³ size, 35g weight and 120 mW power. Microsemi's CSAC product offers ±5.0E-11 accuracy at shipment and a typical ≤ 9.0E-10/month ageing rate, for low power atomic clock holdover applications.

Complete article, here

TSN Ethernet evaluation kit for industrial and automotive applications

Maker of communications-focussed processors and related devices, Innovasic (Albuquerque, New Mexico) has produced a Time Sensitive Networking (TSN) evaluation kit based on its fido5000 REM Switch technology. The kit contains everything needed to evaluate the features of the emerging IEEE TSN standard and is pre-installed with the most mature TSN features starting with 802.1AS and 802.1Qbv. As TSN standards evolve, new features will be made available as free downloads through Innovasic's Developer Portal.

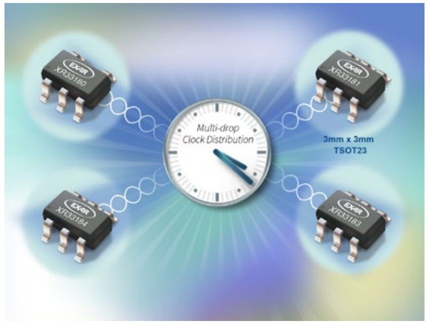


Complete article, here

productroundup

High-speed RS-485 receivers for industrial applications

Offering compatibility with low- voltage logic down to 1.65V and with 52 Mbps data rate, fast propagation delay and low package-to-package skew times for improved operation in clock distribution systems, these receiver chips have ±15kV ESD protection against ESD-related failures. Exar's latest high-speed RS-485/RS-422 receivers feature 52 Mbps data rates, 15 nsec propagation delay and 2 nsec maximum receiver skew. This family is suited for high performance industrial applications such as multi-drop clock distribution, telecom networking, robotic control, and LAN applications.



Complete article, here

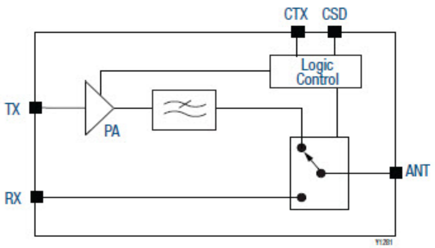
Inova Semiconductors licenses APIX3 to Socionext

Socionext is the first licensee for Inova Semiconductors' latest APIX3 technology, the latest generation of Inova's APIX SerDes (Serializer/Deserializer) technology for in-vehicle video and data communications. APIX3 supports transmission rates of up to 12 Gbps, suiting it for HD and ultra HD infotainment, and ADAS (Advanced Driver Assistance Systems). APIX3 features different operation modes of 1.5 Gbps, 3 Gbps, 6 Gbps and up to 12 Gbps bandwidth, fully supporting HD and UHD displays with touch or gesture control and supporting STP and Coax Cable.

Complete article, here

RF front-end module for smart metering, energy, IoT designs

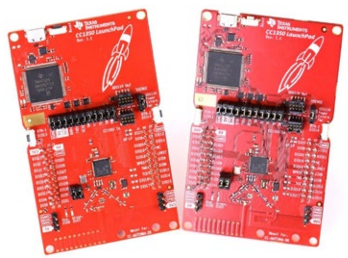
Skyworks has introduced a highly integrated 470 to 510 MHz front-end module (FEM) for smart energy, smart metering (electric, gas, water, heat), security, RFID, industrial and other Internet of Things (IoT) applications in the 470 – 510 MHz range. The SKY66115-11 FEM operates over a range of supply voltages (2.5 to 3.6V) at low power consumption, and comes in a 4 x 4 x 0.9 mm, 16-pin multichip module outline. Its extended range more than doubles when compared to a standalone system-on-chip solution. The device offers transmit output power of +20 dBm.



Complete article, here

Ultra-low power, dual-band wireless microcontrollers from TI

Intended for tasks such as monitoring IoT networks from a handheld device, Texas Instruments' latest series of microcontrollers are single-chip Sub-1 GHz plus Bluetooth low energy ICs. The SimpleLink dual-band CC1350 wireless MCU enables developers to move from a three-chip solution to a single chip, while reducing design complexity, saving power, cost and board space. The CC1350 wireless MCU offers a range of up to 20 km on a coin cell battery. Designed for low-power wide area networks (LPWAN), the CC1350 wireless MCU features dual-band connectivity; a sub-1 GHz network together with Bluetooth low energy.

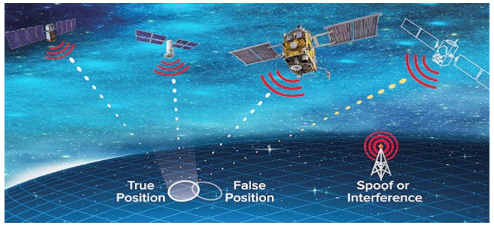


Complete article, here

productroundup

GNSS interference detection identifies PNT system threats

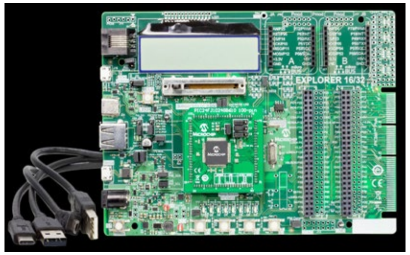
PNT systems – position, navigation and timing – reliant on GNSS signals are increasingly vulnerable to interference, according to Spirent, introducing its GSS200D as the first commercial solution to automate monitoring and analysis of the signal environment. The GSS200D solution comprises field-based hardware and a secure data server for automatic capture and analysis of global navigation satellite system (GNSS) radio frequency interference. Deployments of GSS200D probes readily provide users with a thorough understanding of the RF interference environment at sites of interest.



Complete article, here

Microchip uprates development board for 16-bit and 32-bit PICs

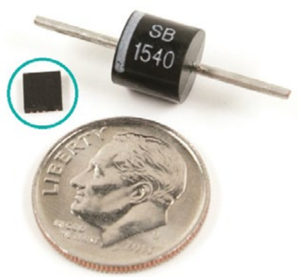
Microchip Technology's Explorer 16/32 Development Board for 16-bit and 32-bit PIC microcontrollers is lower cost than its predecessor Explorer 16 and comes with an integrated programmer/debugger and added features that address the latest embedded systems design needs. It is compatible with the classic Explorer 16 Board. The board is a platform to evaluate the 16-bit PIC24, dsPIC33 and 32-bit PIC32 families of devices through Processor Plug-In-Modules (PIMs) for device swapping. The board features a mikroBUS interface to add new functions using Click Boards from MikroElectronika.



Complete article, here

PV cell string optimizer boosts solar panel output up to 30%

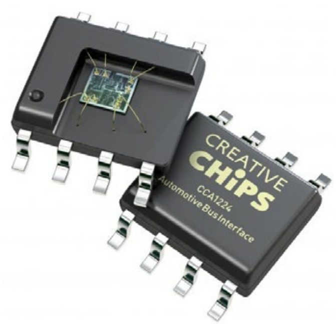
Maxim presents its Cell-String Optimizer as the first IC to perform MPPT (maximum power point tracking) at low level in a panel; it allows photovoltaic (PV) panels to harvest significantly more energy and simplifies design complexity for solar installation projects. Maxim's cell-string optimizers are highly integrated DC-DC converters that replace the bypass diode and perform maximum power point tracking (MPPT) deep inside the PV module. By replacing each diode with a MPPT device, the on-off response to performance mismatch is eliminated; every cell-string contributes maximum power.



Complete article, here

Transimpedance preamplifier ASIC targets optical sensors

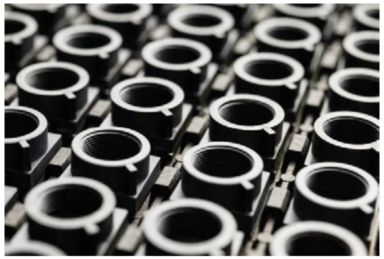
The transimpedance preamplifier circuit CCG1401 from Creative Chips uses a proven BiCMOS technology to achieve excellent noise characteristics for use in optical sensor applications. With only one supply voltage, transimpedance and lower cut-off frequency are programmable via the integrated SPI interface from a connected micro controller. The sensor status is displayed either via a comparator or analogue output. In standby mode the current consumption is only 15µA. A CSP flip chip package is available but the CCG1401 is also offered in a QFN16 package.



Complete article, here

80x80 pixels thermal sensor for large-volume applications

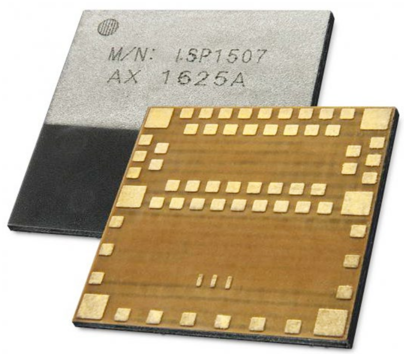
Delivered in a Ball Grid Array (BGA) wafer level package, the fully digital Micro80 Gen2 thermal sensor from ULIS is claimed to be the first infrared sensor box packaged in a JEDEC tray, making it suitable for large-volume applications. The device supports optical fields of up to 120° and is claimed to be the first infrared sensor with a unique plastic lens holder, eliminating the need for OEMs to develop their own. The Micro80 Gen2 consumes less than 55mW and operates in the -40 to +85°C temperature range. It supports a broad spectrum of frame rates (from 1Hz to 50 Hz) and allows vision up to 150 metres.



Complete article, here

Complete Bluetooth LE module shrunk to 8x8x1mm

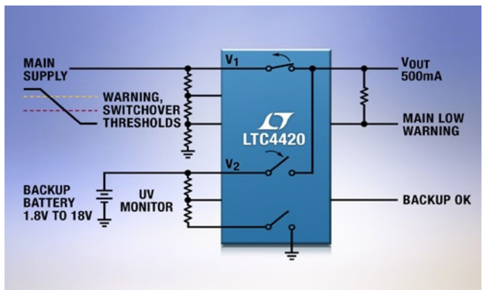
Insight SIP is releasing the ISP1507 to offer Bluetooth Low Energy Technology in a 8x8x1mm System-in-Package. The module integrates Nordic Semiconductor's nRF52832 chip (running Bluetooth 4.2), offering a 32-bit ARM Cortex M4 CPU, 512kB of flash memory, analogue and digital peripherals SPI, I 2C and GPIO. This module forms a fully featured standalone Bluetooth Low Energy node. It draws 5.5mA typical for transmission and reception, 1.5µA in standby mode and 0.7µA in deep sleep mode. Transmission output power reaches +4 dBm and reception sensitivity is -96dBm.



Complete article, here

Monolithic 18V prioritizer manages battery switchover

LTC4420 is a dual input monolithic power prioritizer for 1.8V to 18V systems, designed to enable portability, preserve memory during brownouts, and ensure a graceful shutdown on power loss, in electronic systems employing batteries and capacitors for backup power. The IC normally powers the load from the higher priority main supply such as a wall adapter or battery, switching to the backup supply—typically a battery or large-value capacitor—during primary brownout or power loss conditions. With up to 18V operating capability, the LTC4420 accommodates a wide range of power sources.



Complete article, here

Ultra low, 1microAmp quiescent DC-DC step-down for wearables

Targeted at Li-Ion and coin cell powered devices such as blood glucose meters, remote controls, hearing aids and wireless mouse or other light-load applications, ams has posted details of the AS1313 hysteretic step-down DC-DC converter. The device has a load current capability of 150 mA with an ultra-low quiescent current of 1 µA. The AS1313 is optimized for light loads and with efficiencies of up to 95%. In order to save power it features a shutdown mode, where it draws less than 100 nA. In shutdown mode the battery is not connected to the output.

Complete article, here

5 EMBEDDED SYSTEM CHARACTERISTICS TO KEEP AN EYE ON

BY JACOB BENINGO

No matter how simple or complex the embedded system, there are five key characteristics that developers should monitor closely. A few are obvious, such as RAM and ROM usage. There are others, however, often over looked by developers that can easily become a major sticking point in the design cycle.

Characteristic #1 – System Timing

Ask any developer the minimum, maximum, and average execution times for a system interrupt or other system function and ninety percent of the time the answer will be a blank stare. When it comes to understanding the real-time performance for an embedded system, many developers just cross their fingers and hope for the best. Microcontrollers have become very fast and powerful, but they are by no means a general computing device where timing can be completely ignored. Developers need to understand how their system will respond if, say, multiple interrupts fire simultaneously or if (my favourite test case to try which fails nearly 100% on the first attempt) a user “mashes” all the buttons at once.

Fortunately, modern microcontrollers have available numerous tools that allow developers to understand their system timings and responses. For example, ARM microcontrollers have trace capabilities that allow a developer to sample the PC counter at regular intervals and reconstruct the systems timing and execution path. Utilizing these tools can give developers insights into their system and provide them with real data as to how their system is performing rather than a hope and a prayer that the system is executing code the way a developer thinks it is.

Characteristic #2 – Execution Order

Understanding instruction execution order is just as important to developers as knowing their system timing. It is critical to know where the system is branching or jumping and when and in what order various functions or interrupts are executing. Systems have become so complex that, while we can think we understand what is happening, we need to pull trace data and visually see the code execution. This often reveals a completely different story from what we expected.

I highly recommend that developers investigate and become familiar with their microcontroller’s trace tools. These modern day tools provide visually engaging and insightful diagrams that just weren’t possible a few years ago. I’ve caught so many bugs using the insights they offer that before I write a single line of code I set up my trace and bug trapping tools.

Characteristic #3 – Code Size

Every developer monitors code size: right? I would argue that they don’t, in reality. Most developers, if asked how much code space a GPIO or SPI driver will take on their system, don’t even have a place to go and look for the answer! All they know is that the last application they worked on had GPIO and SPI and the final application used approximately 47 kB of flash space (for example). We are notorious for not tracking the code usage details for our systems.

Now in our defence, code size can vary drastically depending on the compiler used and even the optimization level and flags used. (If you are interested in the potential differences between open source and commercial compilers I recommend checking out Open Source versus Commercial Compilers.) In addition, in most cases today, monitoring code size has become less important because flash is pretty inexpensive and vendors have made it very easy to switch between different parts within the same microcontroller family based on code size. However, it can still be extremely useful to track the details of items such as drivers in order to aid future project planning and part selection.

Characteristic #4 – RAM usage

Rather than code memory, RAM is becoming the crucial factor in embedded software development. It isn't uncommon for microcontrollers to offer flash space exceeding 100 kB but at the same time only offer 16 kB of RAM. This means RAM space is still at a premium. Throw an RTOS in the mix and the situation could quickly become even worse. In an RTOS-based system, it is not uncommon for developers to allocate ungodly amounts of RAM to thread stack space because it is difficult to estimate just the right size. So, as developers create and implement their software, they need to be monitoring where their RAM space is going.

Characteristic #5 – Energy Consumption

Battery operated devices undoubtedly have energy consumption as a key requirement for the system design. But systems that have access to the grid often neglect energy since it isn't a key requirement. Given rising energy costs and limitations in natural resources, though, developers should still continue to monitor their design's power needs to understand what their energy footprint is and how they can minimize the energy they use. With such monitoring, battery operated devices will obviously gain increased operational life between swapping out batteries or recharging the device. Devices that are directly connected to the grid, though, can benefit consumers and end users by saving costs for electricity. Yes, the saving in any idividual case may be minute, but consider a few million devices and suddenly we have a lot of energy no longer being wasted.

Conclusion

These five characteristics need to be monitored by embedded software developers as they create their systems. Modern day systems with substantial resources can sometimes make monitoring these characteristics seem trivial or unnecessary, but at the end of the day the biggest issues I encounter in the field are always related to these five key areas.

***Jacob Beningo** is an embedded software consultant who currently works with clients in more than a dozen countries to improve product quality, cost and time to market. He has published more than 200 articles on embedded software development techniques, is a sought-after speaker and technical trainer and holds three degrees which include a Masters of Engineering from the University of Michigan. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and sign-up for his monthly Embedded Bytes Newsletter.*

EDN europe

EDN-EUROPE is published 11 times in 2016 by
European Business Press SA,
533 Chaussée de Louvain, 1380 Lasne, Belgium
Tel: +32-2-740 00 50 Fax: +32-2-740 00 59
email: info@eetimes.be.
VAT Registration: BE 461.357.437.
RPM: Nivelles.
It is is free to qualified engineers and managers involved in engineering decisions – see:
http://www.edn-europe.com/subscribe

CONTACTS

PUBLISHER

André Rousselot
+32 27400053
andre.rousselot@eetimes.be

EDITOR-IN-CHIEF

Graham Prophet
+44 7733 457432
edn-editor@eetimes.be

Patrick Mannion
Brand Director EDN Worldwide

european business press

CIRCULATION & FINANCE

Luc Desimpel
luc.desimpel@eetimes.be

ADVERTISING PRODUCTION & REPRINTS

Lydia Gijsegom
lydia.gijsegom@eetimes.be

ART MANAGER

Jean-Paul Speliers

ACCOUNTING

Ricardo Pinto Ferreira

SALES CONTACTS

Europe

France, Spain, Portugal
Daniel Cardon
+33 688 27 06 35
cardon.d@gmail.com

Belgium
Nadia Liefsoens
+32-11-224 397
n.liefsoens@fivemedia.be

UK, Ireland, Israel
Nick Walker
The Netherlands
+44 (0) 1442 864191
nickjwalker@btinternet.com

Germany, Austria, Eastern Europe
Victoria & Norbert Hufmann
+49 911 93 97 64 42
sales@hufmann.info

Switzerland
Monika Ailinger
+41-41-850 4424
m.ailinger@marcomedia.ch

Italy
Andrea Rancati
+02 70 30 00 88
arancati@rancatinet.it

Scandinavia
Colm Barry & Jeff Draycott
+46-40-41 41 78
jeff.draycott@womp-int.com
colm.barry@telia.com

USA & Canada

West
Todd A. Bria
+1 831 477 2075
tbria@globalmediasales.com

PA, NJ & NY
Jim Lees
+1-610-626 0540
jim@leesmedia.com

East, Midwest, South Central & Canada
Steve Priessman
+1-630-420 8744
steve@stevenpriessman.com

East, Midwest, South Central & Canada
Lesley Harmoning
+1-218.686.6438
lesleyharmoning@gmail.com

Asia

Japan
Keita Sato
+81-3-6824-9386
ksato@mx.itmedia.co.jp

Taiwan
Laura Chen
+886 2 2759 1366 #305
laura.chen@ubm.com

China
Brandon Smith
+86755 33248168
Brandon.Smith@ubm.com